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Volatile and Non-Volatile Single Electron Memory

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Multi Tunnel Junctions (MTJs) have attracted much attention recently in the fields of Single-Electron Devices (SED) in particular Single-Electron Memory (SEM). In this paper, we have design and study a nano-device structure using a two dimensional array MTJs for Volatile and Non-Volatile-SEM, in order to analyze the impact of physical parameters on the performances. We investigate the single-electron circuit characteristics in our devices qualitatively, using single-electron Monte Carlo simulator SIMON.

Keywords: Single electron memory, Multi tunnel junctions, Quantum dot memories, Write time, Retention time, SIMON.

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1. INTRODUCTON

As the semiconductor device feature size enters the sub-50-nm range, two new effects come into play. One is the quantum effect, which is rooted in the wave nature of the charge carriers, and gives rise to non classical transport effects such as resonant tunneling and quantum interference. The other is related to the quantized nature of the electronic charge, often manifested in the so-called single-electron effect: Charging each electron to a small confined region requires a certain amount of energy in order to overcome the Coulomb repulsion, if the charging energy, $e^2 / 2C$ is larger than the thermal energy k_BT; where C is the island capacitance, T is the temperature, e is the elementary charge and k_B is the Boltzmann constant; a single electron added to the region could have a significant effect on other electrons entering the confined region.

Single-electron transistors (SETs) operate using a Coulomb blockade, which occurs in tiny structures made of conductive material due to electrostatic interactions between confined electrons. There are basically two types of SET application: memory devices [1] and logic functions have been proposed [2]. The small size is especially important for memory devices; memory cells have to be small to achieve a greater degree of integration. Information 'bits' are defined by one, or at most a few, electrons, has found great interest. The single-electron charging and quantum confinement effects into the quantum dot, also lead to stored electrons. To operate the cell with a precise number of electrons by controlling the magnitude of the writing voltage.

In digital electronics, where information 'bits' are defined by one, or at most a few, electrons, has found great interest. The single-electron charging and quantum confinement effects into the quantum dot, also lead to stored electrons

Raising the operating temperature means that we have to reduce the island size of the order of a few nanometers (< 10 nm). Although this is a challenging issue, some devices with multi tunnel junctions (MTJs) have been demonstrated that clearly and conclusively operate at room temperature through the use of recent rapidly developing nanotechnologies. The results provide excellent prospects for the future practical application of SETs.

In this work include three parts. First section is a study of a double structure MTJs, then in second part it an analysis of an N-bit volatile memory with single MTJs, and finally we introduce a novel device for Non-Volatile memory with two MTJs hybrid with a SET.

2. THEORY

2.1 Description

Fig. 1 shows the circuit diagram for a two MTJs with (M-1) islands, and M tunnel junctions in first line, and (P-1) islands, and P tunnel junctions on the second line. The islands are separated from each other and from the source and drain regions, by tunnel junctions with capacitance C_T. The source is connected to the ground. Thus will reduce the error to the order 1 / MP, where M and P are the number of junctions in parallel and in series respectively. For numerical calculations, we used our universal single-electronics simulation program SIMON [3, 4] based on a Monte Carlo approach.

The oxide layer separating the two MTJs is shown in Fig. 1 by a capacitor C_{ox}. Such as approximate expression of the capacity of oxide:

$$C_{ox} = \varepsilon_0 \varepsilon_r S / d$$

The dynamics of the system are governed by the following equation which gives the tunneling rate of an electron in each one of tunnel junctions by using the 'orthodox theory' [5] of single electron tunnelling:

$$\Gamma_{ij} = \frac{1}{e^2 R_T} \frac{\Delta F_{ij}}{1 - \exp(\Delta F_{ij} / k_B T)}, \qquad (2)$$

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where $\Delta F_{ij} = \Delta F_i - \Delta F_j = -eVds$ is the difference between the free energy of the initial and final states, where Vds is the source voltage, and RT is the tunnel resistance. The tunneling rate of global system it is:

$$\Gamma = \sum_M \Gamma^1_{i\to j} \sum_P \Gamma^2_{i'\to j'} \quad (3)$$

where $\Gamma^{1,2}$ denote the first and second arrays respectively. The sum is made on the M and P MTJs.

Experimentally, MTJs with constant values of C and C_{ox} have been fabricated mainly using metal islands [6]. An important property of the two MTJs array is that it can be fabricated with lower resistance, even if it contains many junctions in series. For a good functioning of the structure and to avoid degradation of the system we must choose a high number of junctions.

The charging energy of the island creates an energy barrier which blocks the entrance of electrons into the MTJ so that multistable states of different numbers of electrons can be formed.

The tunneling occurs through one tunnel junction with a simultaneous tunneling of second electron across the same junction is neglected, than the MTJ system is also important in suppressing co-tunneling effects.

When the tunneling through $2M$ ($M = P$) junctions are considered, the effective capacitance C_{eff} at island is given by:

$$C_{eff} = C_i + C_{ox} \quad (4)$$

where

$$C_i = \left[\frac{2M}{2M-1}\right] C_T \quad (5)$$

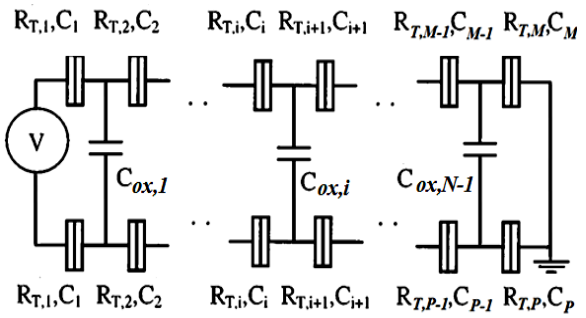

Fig. 1 – A 2D array of tunnel junctions in series. Junction i is characterized by its tunnel resistance R_{Ti} and tunnel capacitance C_{Ti} in parallel and islands have an oxide capacitance C_{oxi}

This may be used to write the potential at the k^{th} island. The effective charging energy, $E_{ch,MTJ}$ is defined similarly to the usual charging energy, except the physical capacitance is replaced with the effective capacitance:

$$E_{ch,eff} = \frac{e^2}{C_{eff}} \quad (6)$$

In an infinity array, the capacitance between two neighboring islands is exactly twice the capacitance of the tunnel junctions, and this is the reason that the offset voltage is a factor of 2 lower in a two arrays compared to a one array.

2.2 Simulation Results

As the bias V increases, the number of transitions in the MTJs increases (Fig. 2). The charge state of the MTJs without any extra electrons may be expressed as $(n_1, n_2) = (0, 0)$. When the applied bias V gives to electron a sufficient energy to tunnels onto the first island he created the state (1, 0). This electron creates a Coulombian barrier energy, forming a zone Coulomb blockade for the other electrons. However, as the applied voltage is increased, other transitions become possible. These additional transitions lead to an increase in the current.

The theoretical results presented give that $C_{eff} = 0.418$ aF; C_{eff} is lower than the total capacitance attached to an island $2C_T + C_{ox} = 0.8$ aF; and $E_{ch,eff} = 0.382$ eV $\approx 14\ k_BT$ ($k_BT = 0.025$ eV at 300 K), this proves that the charging energy is much higher than the thermal energy.

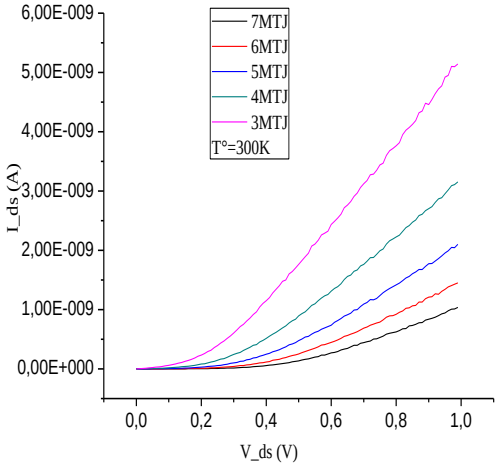

Fig. 2 – Drain current vs. source-drain voltage characteristics at $T = 300$ K in two MTJ arrays, with $C_T = 0.2$ aF, $C_{ox} = 0.2$ aF and $R_T = 40$ MΩ

Therefore increase the number of tunnel junctions network can overcome the effect of low capacity and temperature operating. The staircase is typically irregular, with variation in the step heights and widths. The blocking region is more important, also when the number of junctions increases for 2×7 MTJs. The threshold voltage is 0.3 V, and from the curve it is ~ 0.4 V. The current Ids it changes from ~ 1 nA (7 MTJs) to ~ 5.2 nA for 3 MTJs.

Also, the tunneling rate of global system has a new factor so that: $\Gamma^* = \alpha \times \Gamma$ where α is factor which depend on the effect of coupling capacitor.

In general, when the stray capacitances increase, the I-V curve of the single-electron device is shifted towards the low-voltage side [7, 8] when the stray capacitances increase.

The conduction current is activated at higher temperatures even at low temperature, and the I-V curve is not looks Ohmic attitude (Coulomb blockade

region). Also the increase in the temperature increase the conductivity and this due to excited states of the array that are thermally populated, which contribute to the current. Single-electron current oscillations are observed in the Ids vs. Vgs characteristics Fig. 3 without degradation like we have a simple SET, the oscillations persist up to 300 K with an unchanged period.

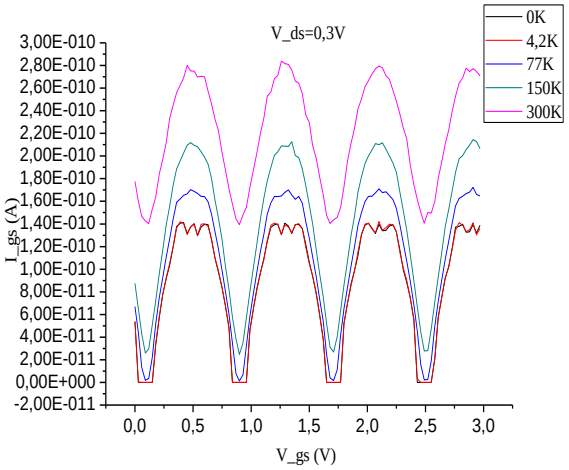

Fig. 3 – Periodic single-electron oscillations in the Ids-Vgs characteristics of two dimensional arrays with $M = P = 6$ at a constant value of $V_{ds} = 0.3$ V as Temperature is varied

For the applications of that structure, such as the multiple value logic (MVL) circuits [9] and logic memory circuit, we need to have a gate or multi-gates allows more than two levels of logic. So we have added to the circuit in the Fig. 1, two gates for each array; generally the two gates, one gate is used as voltage input port and the other gate is used as threshold voltage adjusting port.

3. MEMORY APPLICATION

3.1 Volatile Memory with One MTJ Array

3.1.1 Description

Volatile single-electron memory (V-SEM) can be realized by using a one MTJs arrays, is shown in Fig. 4, in fact the substrate is modeled by a capacity C_{sub}, $u_1 \ldots u_7$ are the input and erase operation of V-SEM, each island is the center of memorization. All tunnel junctions of MTJs are identical. In Fig. 5b, we present the memory dot charges q results for the one-dimensional random array of seven metallic dots separated by eight tunnel junctions at 4.2 K. Tunnel capacity are chosen such as $C_T = 0.13$ aF and the tunnel resistances as $R_T = 40$ MΩ. The normal capacity are substrate-capacity $C_{sub} = 2$ aF and gate-capacity $C_G = 0.2$ aF. The effective total capacitance is given by

$$C_{eff} = \sqrt{C_G^2 + 4C_T C_G} \tag{7}$$

The total capacitance of an SET with a single island is given by $2C_T + C_G$ (about 0.4 aF in this case) contrariwise the effective total capacitance C_{eff} is 0.202 aF of the MTJs is about half this value and the operation temperature becomes two times higher by multiplexing islands. The stability of device requires that the capacity of the substrate is greater than the capacity of the gate and tunnel junctions, otherwise the memorization in each island becomes uncontrollable and storing voltage varies from island to another.

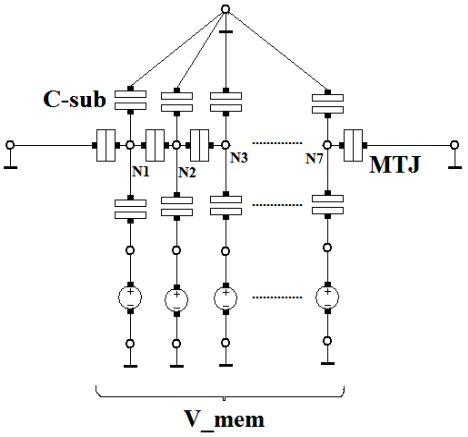

Fig. 4 – Schematic circuit of the basic volatile single-electron memory cell

3.1.2 Operation

We assume that the device does not exhibit any memory or excess charges. The applying voltage (inputs voltage) V will inject an electron into the MTJ, and a current begins to flow. The threshold voltage when this occurs is given by:

$$V_{th} = \frac{e}{2C_{eff}} \tag{8}$$

In our case $V_{th} \approx 0.4$ V when $V_{mem} > V_{th}$, the applied potential V to the node Ni will lower his energy level and holds the trapped charge confined

The inputs voltage (Fig. 5a) can take two values 0 V, which correspond to the logic "0" and 0.6 V, which correspond to the logic "1". The presence of an excess electron at Ni corresponds to logical "1" and the absence to logical "0". If only the applied input u1 takes the values 1 V the charge of N1 is one electron (one bit) and the other nodes equals to zero ($u_2 = u_3 = \ldots = u_7 = 0$ V). Generally if some inputs equal to 0.6 V then the corresponding node represents the logic "1" from where the devices is called multi-bit memory. All combinations of logic "0" and "1" are possible in the device i.e. "1","0","1","0","1","0","1" or "0","1","0","1","0","1","0" etc.

In the case of logic "0", should be applied a low voltage of about 0.08 V to 0.1 V in order to maintain the energy level of node uncharged stable avoid the perturbation due of its neighbor charged.

The thermal energy (~ 0.025 eV at 300 K) compared with the charging energy we find that $E_{ch} = 0.39$ eV ~ 15 k_BT, this will improve the room temperature operation. Fig. 5c show the simulation result of device at 300 K, so the temperature does

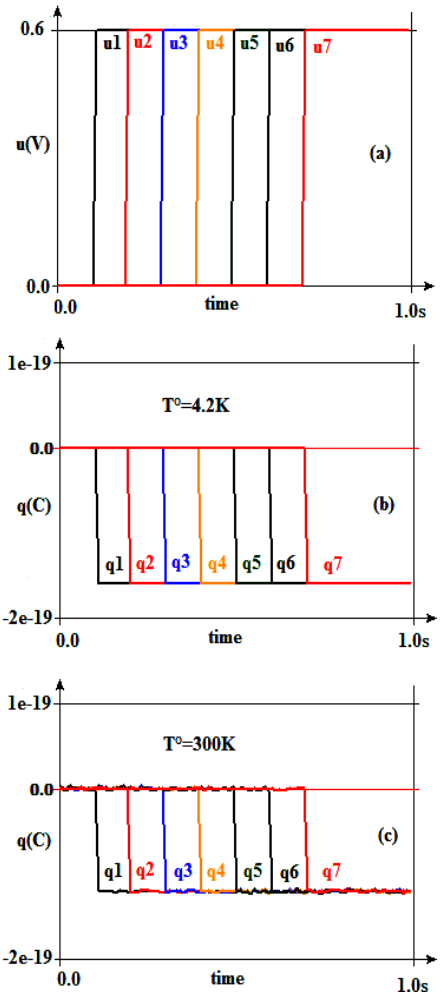

Fig. 5 – (a) Time variation of the memorization voltages ($u_1 \ldots u_7$) Time variation of the charge ($q1 \ldots q7$) at the output nodes $N_1 \ldots N_7$, (b) at 4.2 K and, (c) at 300 K

not effect on the functioning of devices but on the voltage memory. For the high temperature it must be multiplied V_{mem} by two.

To pass from the state "1" to "0" it is sufficient that V_{mem} remains at 0V; the operation is simulated in Fig. 6 at low and room temperature. When $u_1 = 0$ V, the excess electron in N_1 is transported to the ground and not to N_2 although $E_{F1} > E_{F2}$, the Coulomb blockade it prevented.

The simulation results of substrate current shows that it null evidence that the electron transfer is not across the substrate. The electron is transported from the ground to the nodes N_i.

3.1.3 Energy and Transport

If inputs voltages are set to 0 V the Fermi energy levels of each node are all above the level of E_F of ground; coulomb blockade. We should also note that the energy levels of the islands are not equal since of electrostatic repulsion exist in the system, (Fig. 7a). Where $u_1 = 1$ V so $EFN_1 = EF$, the coulomb blockade is suppressed an electron can pass to node N_1 but not to N_2 since the condition $EFN_2 > EFN_1$; coulomb blockade. For $u_2 = \ldots = u_7 = 0.6$ V then an electron moves from the first node to the other nodes since all energy levels are aligned, (Fig. 7b).

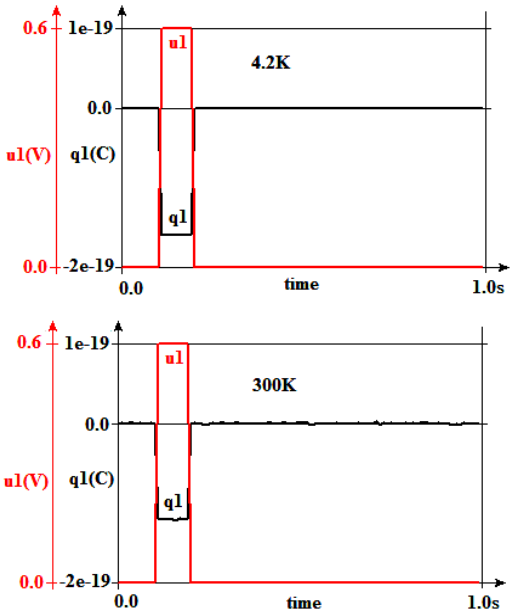

Fig. 6 – Erase operation for the node N_1 at 4.2 K and 300 K

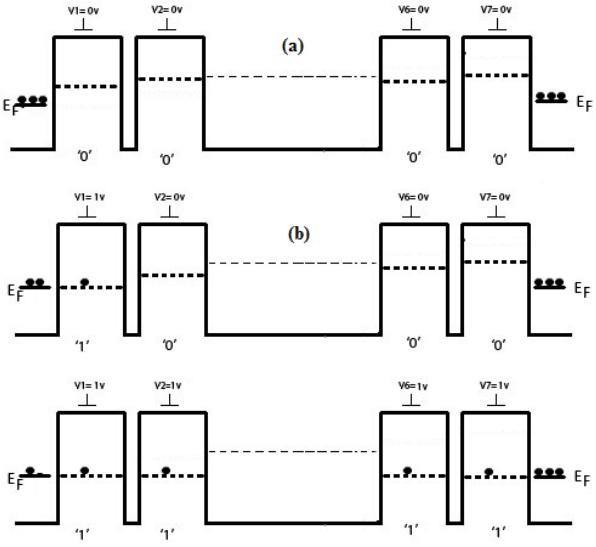

Fig. 7 – Energy diagram of the system, (a) for logical "0" (b) logical "1" in node N_1 and for all nodes

The free energy of the system reaches a local minimum therefore the presence of an electron in N_1, $N_2 \ldots N_7$ (the node are indicated by the numbers 1...7 in Fig. 7). When the electron is transported only from the right (or left) ground we can note that there are 28 tunnel events (Fig. 8b) and the free energy tend to 0.4 eV but if the tunneling effect is in both directions it was 16 events (Fig. 8a).

The system is more stable in a unidirectional tunneling because the energy levels occupied by electrons in seven nodes, are separated and tends to neglect the electrostatic interactions. So that proves one unidirectional transfer.

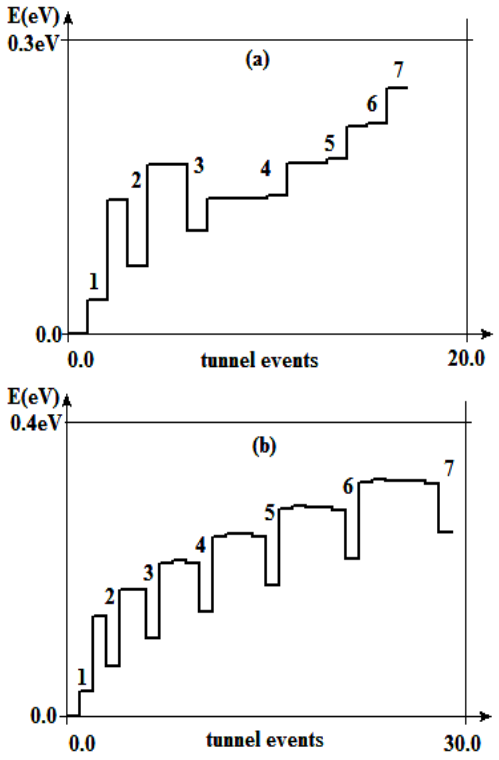

Fig. 8 – Free energy history of transition from logic "0" to "1"of overall system, (a) the tunnel effect is in both directions and (b) tunneling is in one direction

3.2 Non Volatile memory with Two MTJs Arrays

3.2.1 Description

We now consider a Non-Volatile single-electron memory (NV-SEM) circuit, the principal parts of basic circuit schematic is shown in Fig. 9, which consists of the two MTJs cell coupled with a simple single-electron transistor. This idea is based on the electron-trap memory cells was proposed in [10, 11].

The charged state and the uncharged state on the memory-dot can be used to represent binary information "1" and "0". SET, is used to control the charging of the memory node (write and erase operations). The write operation is sensed in the current of the MTJs (read the information).

The current through the SET will be sensitive to the number of electrons in memory-node. Each MTJ array has 6 tunnel junctions coupled by an oxide layer. The resistance of each one of these junctions is 40 MΩ and the capacitance 0.2 aF. For the SET parameters is defined by: $R_D = R_S = 40$ MΩ, $C_D = C_S = C_g = C_S = 2.10^{-19}$ F $C_C = 2.10^{-18}$ F. Where C_S is the substrate capacity and CC is the coupling capacity.

By applying a positive voltage V_{ds} or V_{gs}, so if the energy can provide the Coulomb blockade energy an electron or a small number of electrons is transported from the ground to island. When the writing voltage increases, the number of electrons on the memory node can be changed. The energetic of the Coulomb blockade in the array of single-electron memory cells make it possible to enable and disable certain single-electron.

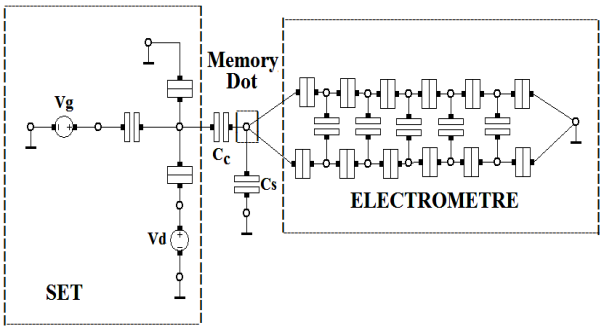

Fig. 9 – Schematic circuit of the basic non volatile single-electron memory cell

3.2.2 Writing

The simulated operation of the memory cell is shown in Fig. 10. So, the first electron will enter the array only when it becomes energetically favorable. When the polarization V_{ds} increases from 0 V to 1.6 V it was stored four electrons in the island. The probability error of finding N electrons in the quantum dot is then given by:

$$P_{err} = \text{constant} \times e^{-t/\tau} \tag{10}$$

Here τ the time required to charge-up the memory node can be approximated with the previous data as:

$$\tau = R_T C_T \tag{11}$$

From previous data the write time is $\tau \approx 16$ ps.

The probability for a bit error has to be below 10^{-20}, then we get $t = 46\ \tau$, therefore one must wait about 0.46 ns for a tunnel event. This approximation is very close to the result given by SIMON shown in Fig. 10.

3.2.3 Detection

Initially, the voltage V_{ds} is zero and there are no excess electrons at the memory-node. After 0.4 ns V_{ds} becomes reaches the value of 0.5 V. At this time an electron is transported from the ground and stored under the effect of Coulomb blockade, this causes the positive current pulse in each MTJs (Fig. 11), so the tunnel junctions MTJ1 and MTJ2 are used as a sense parts to detect the memory-node charges. Each trapped electrons represents a positive peak of current in one of two arrays junctions. Let us note that there are no predictions which of the two junctions will have be an electron transfer.

If the magnitude of the write pulse function is less than $C_\Sigma V_{th} / C_g$, then no electrons are written to the memory. During a positive write pulse, the voltage across the MTJ to be greater than $V_C = Q_{dot} / C_\Sigma$ causes change to the state of the memory. During a negative write pulse, the stored electrons are removed from the memory node via the MTJ.

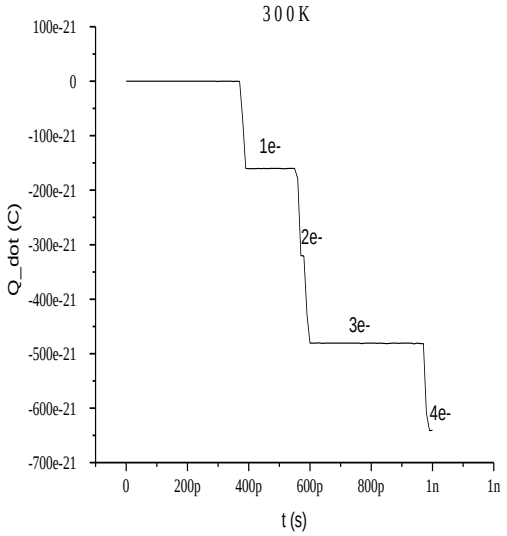

Fig. 10 – Time evolution of the charge in the dot of memory for 1 ns

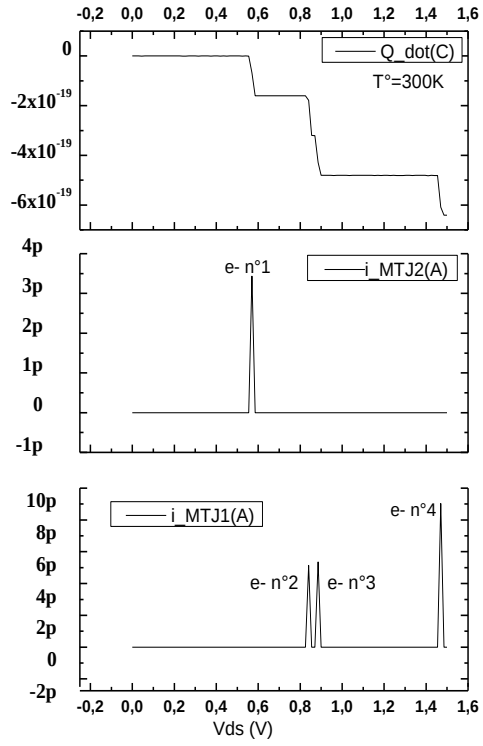

Fig. 11 – Detection of memorized electrons from currents peaks in each array junctions

3.2.4 Temperature effect

There is a critical temperature T_c above this temperature the electrons can be stored in the node. The memory-node storage depends both on the voltage applied to the gate/source-drain, and on the temperature. Fig. 12 proved that the thermionic effect playing a very important role in the memory effect of the structure. The write of the logic "1" start at $T_c = 256$ K. The fluctuation of charges begins when T is near to the critical temperature, and for temperatures below than T_c, no memory effect.

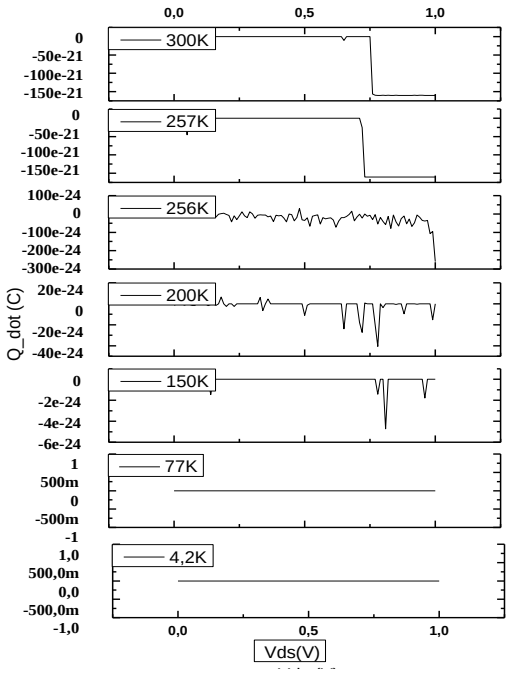

Fig. 12 – Charge evolution in dot-memory as function of temperature

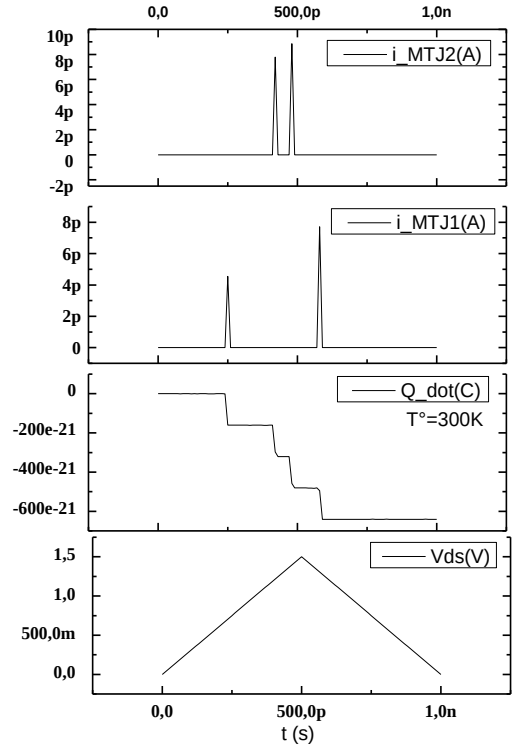

Fig. 13 – Retention of 4 electrons in memory dot

More the oxide thickness decreases, the tunnel current density increases. The reduction of the barrier due to high temperature, promotes the passage of electrons by Tunnel or/and Fowler-Nordheim tunneling in the case of thick oxide (> 10 nm) [12]. The reduction of the barrier leads to a decrease in the effective length of the potential barrier that must cross the particle and thus to increase the "probability of passage".

3.2.1 Retention of cell

Now consider our memory structure and see what happens if the polarization returns to zero? It is clear in Fig. 13 that four electrons are kept off in the memory-node. Katayama et al. [13] derived a simple expression for the retention time of the cell:

$$t_{1/2} \approx \frac{R_T C_S C_\Sigma}{eQ_{dot}} k_B T \exp\left(\frac{eQ_{dot}}{2k_B T C_\Sigma}\right) \quad (12)$$

where $t_{1/2}$ is the time taken to lose half the stored charge Q_{dot}, we can found for 4 electron that $t_{½} \approx 1$ s.

4. CONCLUSIONS

During this work we studied the structure with at multiple tunnel junctions are shows that this way of inquiry is less sophisticated as well as applications of great value for memories component. The study and analysis of logical memory based on single and double MTJs arrays show that a one MTJ array can be used for a multi-bit volatile memory and we demonstrate that electron transfer is in one direction, then we prove that the hybrid SET with two MTJs may result to a non-volatile memory and that works only for high temperatures with a duration of retention greater than 1 second.

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