

## Memristor Effect in Ni/TiO<sub>x</sub>/p-Si/Ni and Ni/TiO<sub>x</sub>/p-Si/TiO<sub>x</sub>/Ni Heterojunctions

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In present work we developed new memristive devices of sandwich-type Ni/TiO<sub>x</sub>/p-Si/Ni and planar one Ni/TiO<sub>x</sub>/p-Si/TiO<sub>x</sub>/Ni. A pinched hysteresis loop is observed for both device configurations and depends on supplementary illumination by UV/visual light. Besides classical model of migration of oxygen vacancies in titanium oxide we considers the impact of barrier modulation and recharging of surface states in TiO<sub>x</sub>/Si interface when voltage is applied to the structure in the dark or under illumination. The elaborated heterostructures show great potential as a low cost material for embedding memristive memory for large area electronics, compatible with Si CMOS process and can be managed by external illumination.

**Keywords:** Memristor, Titanium oxide, Schottky barrier, Surface electronic states

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### 1. INTRODUCTION

A memristor is a passive electronic element that displays a pinched hysteresis loop in its current-voltage (I-V) characteristics. All 2-terminal non-volatile memory devices like resistive random access memory (RRAM) based on resistance switching are memristors, regardless of the device material and physical operating mechanisms. They all exhibit a distinctive “fingerprint” characterized by a pinched hysteresis loop confined to the first and the third quadrants of the I-V curves whose contour shape in general changes with both the amplitude and frequency of input voltage. In particular, the pinched hysteresis loop shrinks and tends to a straight line as frequency increases [1, 2]. The memristor was originally proposed in 1971, the actual fabricated devices exhibiting the characteristics of the memristor were created from 2008 [3, 4].

The first memristor concept was based on the metal-insulator-metal (MIM) structures in which the layers of metal oxides like titanium dioxide are used. Dielectric layer is fabricated with a conductive doped region and an insulating undoped region between 2 metal electrodes [5]. The device is bipolar (the currents in opposite directions reveals opposite effects) and it is also nonvolatile (the resistance state would persist even after the current ceased). Later a series of new memristor concepts were described. Among them it was proposed device as a cylinder of insulating oxide with a narrow conductive channel down the middle; current flowing through the channel heats the cylinder from the inside out, causing a phase transition that converts surrounding layers of material to the conducting state. Specifically, the heating induces a Mott transition, in which localized electron clouds begin to overlap, bringing on a sudden increase in conductivity [6, 7].

Now there is strong interest in creating new

memristive devices due to their significant impact in many fields including digital information systems, analogue circuits and artificial neural networks as a new class of fundamental electronic elements.

In present work we develop the memristive device based on metal/TiO<sub>x</sub>/silicon structure. Two switching-on configurations have been realized – sandwich-type and planar one.

### 2. EXPERIMENTAL

The experimental samples were made on the boron doped (100) Si with resistivity of 10 Ω·cm. Porous TiO<sub>x</sub> film of about 200 nm thick was created on the face side of silicon plates using a method of vacuum thermal evaporation from TiO<sub>2</sub> powder. AFM image of obtained film shows that titanium oxide is mesoporous with average dimension of few tens of nanometers. Ni of about 1 mm thick was deposited as rear Ohmic contact. After that, series of front round contacts (with the distance between centres of 5 mm) and the diameter of 2 mm were deposited on the top of oxide layer. DC magnetron sputter deposition in Ar from metallic Ni target through a steel mask was used.

At the measurement of I-V characteristics the voltage sweep included three consecutive phases: 1) from zero to maximal positive potential on rear Ohmic contact (for sandwich-type switching) or second probe (for planar-type switching); 2) from maximal positive potential to maximal negative potential; 3) from maximal negative potential to zero. And there was no any special delay between these three phases. All I-V curves were obtained at total durations of sweep from 15 ms to 4 min.

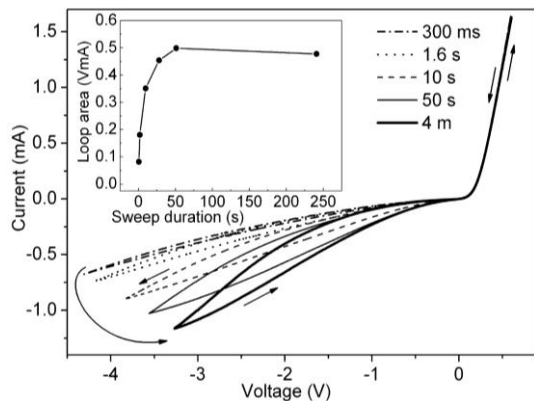
As a source of light, 50 W tungsten filament halogen lamp was applied. To reveal spectral sensitivity of the samples, three optical filters with various transmittance bands were placed between the light source and

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the samples consecutively: red/IR (610-2600 nm), green (480-600 nm) and UV (280-380 nm).

### 3. RESULTS AND DISCUSSION

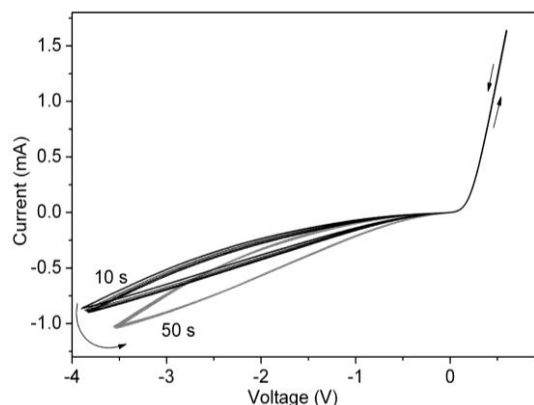
I-V characteristics of the sandwich-type switching, measured in darkness at different durations of external voltage sweep are shown in Fig. 1.



**Fig. 1** – I-V characteristics for sandwich structure measured in darkness at sweep durations of 300 ms, 1.6 s, 10 s, 50 s and 4 min. Insert shows hysteresis loops area vs sweep duration

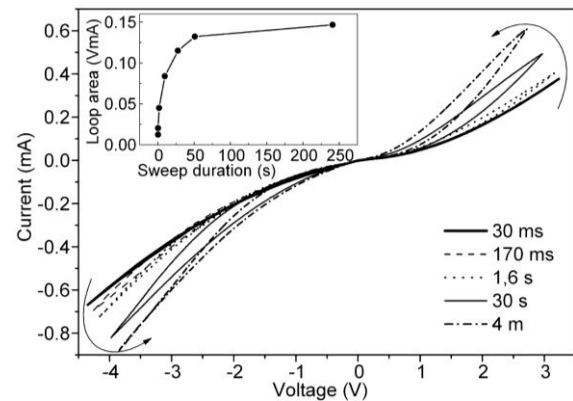
The arising of pinched hysteresis loops on I-V curve indicates the memristor-type behavior. However, in contrast to classical memristive device, the loops are observed only at third quadrants of the I-V characteristics (reverse I-V curves). The absolute value of reverse current grows with the increasing of sweep duration. In forward direction the value of current did not depend on sweep duration. Besides, as it is typical attribute for memristive devices, the decrease of duration sweep results in collapse of pinched hysteresis loops area.

As can be seen the hysteresis loops area increases up 1 order at increasing of duration sweep from 300 ms to 50 s, and then it is saturated (Fig. 1, insert). Crossbar of device shows switching ratio  $\sim 2$ , that is the same value like for other metal oxide memristive devices [8]. No significant degradation of the device was observed when 3 months old devices were tested or at consecutive I-V measurements indicating the good stability and reproducibility (Fig. 2).



**Fig. 2** – I-V curves for sandwich structure measured in darkness at sweep durations of 10 s (10 consecutive measurements) and 50 s (5 consecutive measurements)

In contrast to sandwich structure the bipolar resistive switching is demonstrated in the case of planar configuration (Fig. 3). Again, the decrease of duration sweep results in collapse of hysteresis loops area, the last increases up to duration sweep of 50 s, then it is saturated (Fig. 3, insert). The value of currents and hysteresis loops are approximately the same for 1 and 3 quadrants.



**Fig. 3** – I-V characteristics for planar structure measured in darkness at sweep durations of 30 ms, 170 ms, 1.6 s, 30 s and 4 min. Insert shows hysteresis loops area vs sweep duration

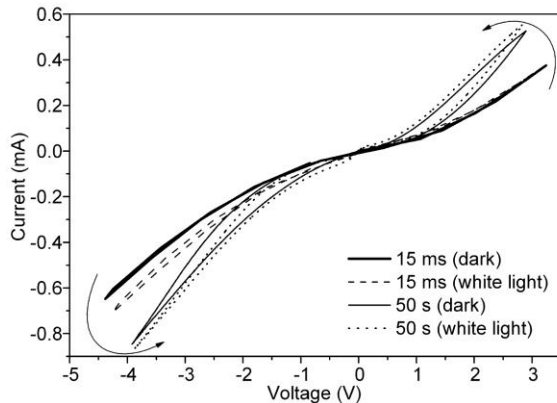
The well-known  $\text{TiO}_2$  memristor model implies that switch the memristor between conducting and insulating states is due to the shift of boundary between the doped and undoped regions at voltage applying. The moving of boundary between two sublayers under application of external bias can be explained by migration of oxygen vacancies in  $\text{TiO}_2$ . This process leads to change of common resistance of nanostructure, depending on charge flowed through the sample [4].

However, the consistent use of this model to explain the observed results meets certain difficulties. Both sandwich ( $\text{Ni}/\text{TiO}_x/p\text{-Si}/\text{Ni}$ ) and planar ( $\text{Ni}/\text{TiO}_x/p\text{-Si}/\text{TiO}_x/\text{Ni}$ ) devices does not contain the special doped and undoped titanium oxide sublayers, but reveals the behavior of memristor-type. Accounting the millimeters distance between metal electrode for planar structure, the hundred of nanometers thickness of  $\text{TiO}_x$  layer, even possible deviation from the bulk  $\text{TiO}_x$  composition in the near contact region may not cause such magnitude of the effect as observed in the experiment. Hence, it is possible to assume that the observed memristor effect is not associated only with the migration of oxygen vacancies in  $\text{TiO}_2$ . Obviously, that the observed current increasing at supplementary illumination by white light on I-V curve of planar (Fig. 4) and sandwich structures cannot be explained by migration of oxygen vacancies in  $\text{TiO}_x$ .

Small difference in the values of the currents with the same voltage applied to both types of structures suggests that the current flow in the planar structure is on the way  $\text{Ni}-\text{TiO}_x-p\text{-Si}-\text{TiO}_x-\text{Ni}$ . That is, as for the sandwich structure  $\text{Ni}/\text{TiO}_x/p\text{-Si}/\text{Ni}$  the memristor effect is related to the properties of the titanium oxide – silicon interface. It can be the recharging of surface states in interface  $\text{TiO}_x/\text{Si}$  or modulation of potential barrier in metal-oxide-silicon contact during the slow reverse voltage supply. Such model is considered in [9] in which the volatile resistive switching effect at a prototypical Schottky metal/oxide interface was reported and was realized a family of transition-metal-

oxide memristors showing distinct hysteresis characteristics based on the interface.

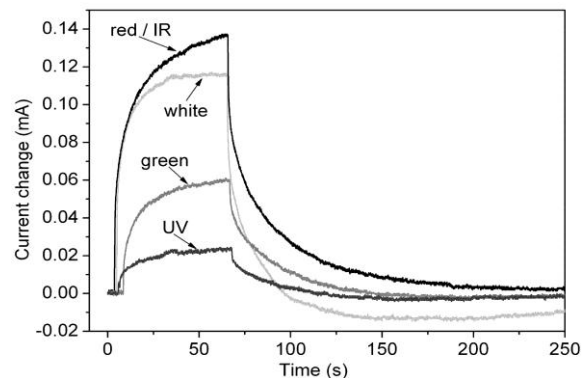
Although the generation of defects in the active layer of titanium oxide was found when it is irradiated by UV light [10] the observed effect of light on the I-V characteristics (Fig. 4) is, likely, to be associated either with the recharge of surface states at the titanium oxide - silicon interface or the absorption of light in Si substrate which reduces the series resistance.



**Fig. 4** – I-V characteristics for planar structure measured in darkness and at illumination by white light of halogen lamp at sweep durations of 15 ms and 50 s

As can be seen from Fig. 5 the pulse illumination of sandwich structure results in slow photocurrent exponential increasing/decreasing with time of ten of seconds. Such large photoconductivity decay and photocurrent generation time are not typical for silicon wafers [11]. Before we studied *p*-Si/porous TiO<sub>2</sub>/Pd structure by the method of Deep Level Transient Spectroscopy (DLTS) [12]. It was found that the DLTS spectra contain at least two characteristic peaks which appear at the lower temperatures with activation energy 0.4

and 0.45 eV. Deep electronic traps in porous titanium oxide with activation energy 175-375 mV were observed in thermostimulated polarization measurements [13]. These electronic traps are responsible for the effect of the negative differential conductivity in the heterojunction based on porous TiO<sub>x</sub> observed at room temperature. The negative differential conductivity disappears after the supplementary UV/vis illumination. However, in general, it should be noted that further studies are needed to clarify the mechanisms of memristor effect in mentioned structures.



**Fig. 5** – Kinetics of photocurrent for sandwich structure at different illumination and  $V = -1.85$  V

#### 4. CONCLUSION

The elaborated memristive devices based on planar Ni/TiO<sub>x</sub>/*p*-Si/TiO<sub>x</sub>/Ni and sandwich structure Ni/TiO<sub>x</sub>/*p*-Si/Ni shows the pinched hysteresis loops which can be managed by external illumination. The elaborated heterostructures shows great potential as a low cost material for embedding memristive memory for large area electronics, compatible with Si CMOS process.

#### REFERENCES

1. L. Chua, *Appl. Phys. A* **102**, 765 (2011).
2. J.P. Strachan, J.J. Yang, L.A. Montoro, C.A. Ospina, A.J. Ramirez, A.L.D. Kilcoyne, G. Medeiros-Ribeiro, R.S. Williams, *Beilstein J. Nanotechnol.* **4**, 467 (2013).
3. R. Williams, *IEEE Spectr.* **45**, 28 (2008).
4. D.B. Strukov, G.S. Sinder, D.R. Stewart, R.S. Williams, *Nature* **453**, 80 (2008).
5. W. Wang, C. Yakopcic, E. Shin, K. Leedy, T.M. Taha, G. Subramanyam, *2014 National Aerospace and Electronics Conference (NAECON 2014)*, 259 (Dayton: IEEE: 2014).
6. A.S. Alexandrov, A.M. Bratkovsky, B. Bridle, S.E. Savel'ev, D.B. Strukov, R.S. Williams, *Appl. Phys. Lett.* **99**, 202104 (2011).
7. D.B. Strukov, F. Alibart, R.S. Williams, *Appl. Phys. A* **107**, 509 (2012).
8. Z.J. Chew, L. Li, *Mater. Lett.* **91**, 298 (2013).
9. M. Yang, N. Qin, L.Z. Ren, Y.J. Wang, K.G. Yang, F.M. Yu, W.Q. Zhou, M. Meng, S.X. Wu, D.H. Bao, S.W. Li, *J. Phys. D: Appl. Phys.* **47**, 045108 (2014).
10. V.A. Skryshevskyy, Th. Dittrich, J. Rappich, *phys. status solidi a* **201**, 157 (2004).
11. S.N. Singh, R. Gandotra, P.K. Singh, B.C. Chakravarty, *Bull. Mater. Sci.* **28**, 317 (2005).
12. V.A. Skryshevskyy, V.A. Vikulov, O.V. Tretiak, V.M. Zinchuk, F. Koch, Th. Dittrich, *phys. status solidi a* **197**, 534 (2003).
13. A.I. Manilov, A.M. Veremenko, I.I. Ivanov, V.A. Skryshevskyy, *Physica E* **41**, 36 (2008).