JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **9** No 4, 04018(4pp) (2017)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **9** № 4, 04018(4cc) (2017)

Comparative Analysis of CNTFET and CMOS Logic based Arithmetic Logic Unit

K. Nehru*, T. Nagarjuna†, G. Vijay‡

Department of Electronics and Communication, Institute of Aeronautical Engineering, Hyderabad, India

(Received 18 April 2017; published online 27 July 2017)

This paper proposes the novel low power and area efficient ALU (Arithmetic and Logic Unit) using adder and multiplexers. The adder and multiplexer are realized by using CNTFET (Carbon Nano Tube Field Effect Transistor) A verilog model of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) in cadence spice software. The proposed ALU is simulated using Monte carlo simulation at 0.9 sub threshold voltage tested with 45 nm technology for the measurement of power and transistor counts. The power consumption of CNTFET based ALU is found to be 45.67 % better than the existing technologies.

Keywords: CNTFET, ALU, CMOS, MOSFET, Verilog, CPL.

DOI: 10.21272/jnep.9(4).04018 PACS number: 85.30.Tv

1. INTRODUCTION

The low power consumption is achieved by several techniques at different levels like algorithmic level, architecture level and circuit level. The impact on channel length over threshold voltage on performance characteristics of transistors was addressed in [1]. By Scaling down the feature size of CMOS technology, many challenges appear. Lithography limitations, large parametric variations, high power density are some of these critical challenges. To overcome these difficulties and challenges in sub-nanometer scale new technologies have emerged [2]. A carbon nano tube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nano tube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. The exceptional electrical properties of carbon nano tubes arise from the unique electronic structure of graphene itself that can roll up and form a hollow cylinder [3]. The main difference between a CNTFET and a MOSFET is the channel, in CNTFET the channel comprises of one or more carbon nanotubes depending on the channel current requirements whereas in the MOSFET the channel is made of bulk silicon. The CNTFET is a definite alternative to the existing MOSFET. If $n = m$ then the CNT is metallic or else it is semiconducting in nature [4]. The diameter of a CNTFET is obtained from chiral vector as

$$D_{CNT} = \frac{\sqrt{3}a\left(\sqrt{n^2 + m^2 + mn}\right)}{\pi} \quad (1)$$

here $a = 0.143$ nm is the carbon – carbon atomic spacing. From the equation above (1) for diameter of a CNTFET it can be observed that by changing the chiral vector the diameter of CNTFET can automatically be changed. The ternary logic as better choice for area concern and carbon nanotube field effect transistors (CNTFET) are used to improve the performance of the device [5]. In most of the modern design is based on Carbon nanotube because of its superior properties in terms of power consumption, leakage power, delay. The quantum capacitance has a significant force in nanoscale device [6].

The CNTFET-based 8T SRAM cell demonstrates that it provides high stability, low delay and low power, which is better than CNTFET-based 6T SRAM cell as well as CMOS SRAM cell was addressed in [7]. The low power Viterbi decoder is designed with the help of carbon nano tube field effect transistor. The Viterbi decoding is important key element in designing error correction code for digital The challenges and issues of analog design was addressed in [8]. Current mirrors are essential for biasing, amplification and level shifting in analog circuit design [9]. The behavior of carbon nanotube field effect transistors (CNTFETs) under non-ballistic conditions and based on the changes of gate dielectric constant the performance of CNTFETs has been explored in detail as a function of temperature [10]. The design of transmission gate using am bipolar logic in CNTFET technology gives full swing restoration voltage at the output node. The electron and hole mobility of CNT is equal. This feature is useful for realizing logic gates with minimum area [11].

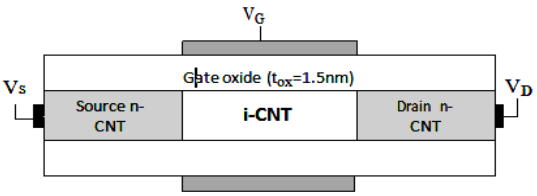

Fig. 1 – Cross sectional view of CNTFET devices

The cross sectional view of CNTFET is shown in Fig. 1. The static DCVS-based standard ternary gates (Inverter/ Buffer, AND/NAND, OR/NOR), which are fundamental components of every arithmetic or logic units, are proposed with the use of CNTFET technology [12]. Minority function is utilized in the voting systems for decision making and also it is used in data mining [13]. The threshold voltage of the intrinsic CNT channel can be approximated to be of first order as the half band gap is an inverse function of the diameter [14-15].

* nnehruk@gmail.com
† Nagarjuna473@gmail.com
‡ Gpvijay24@gmail.com

2. CONVENTIONAL FULL ADDER TOPOLOGIES

2.1 Data Path Element

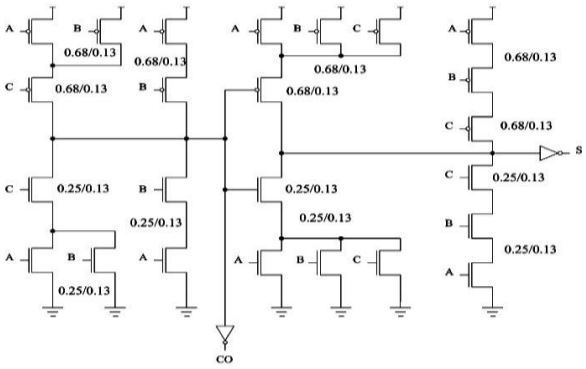

Fig. 2 – Data path element for ALU (one bit addition)

Fig. 2 shows the transistor level schematic of the one bit static CMOS full adder circuit. The main advantage of static CMOS full adder is its ability to produce full swing voltage. The main drawback of static CMOS adder is, it requires more transistors for arithmetic operations it results in capacitive effect [16].

2.2 Level Restoring PTL for One Bit Addition

Fig. 3 shows the transistor level schematic of the one bit level restoring PTL full adder circuit. The drawback of this logic is, it occupies more area and sizing of transistor is very important in this design. This circuit consists of 32 transistors [16].

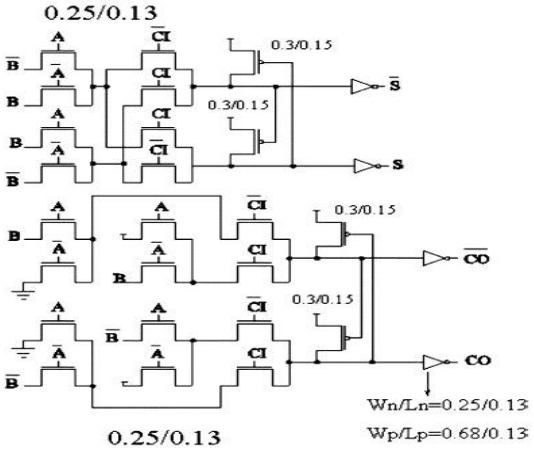

Fig. 3 – Level Restoring PTL for one bit addition

2.3 One Bit Addition Using LP Modulo 2 Addition and Equalizer Gates

2.3.1 LP Modulo 2 Addition and Equalizer Gates

Fig. 4 (a) and (b) shows the transistor level schematic of the 2 input LP modulo 2 addition and equalizer gates. For the LP equalizer gate good logic levels are obtained for input signals. The best case combinations are 00, 01, 10 and the worst case combination is 11 [16].

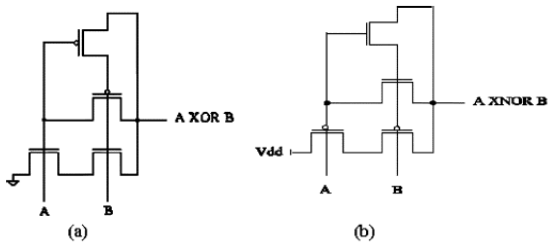

Fig. 4 – (a) LP modulo 2 addition Gate, (b) LP equalizer Gate

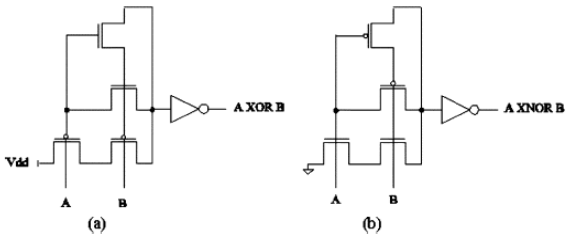

Fig. 5 – (a) LP modulo 2 addition Gate, (b) LP XNOR Gate with Driving Output

In order to enhance the driving capability, CMOS inverter is used at the output nodes, as shown in Fig. 5. By using the LP modulo 2 addition and equalizer gates, the sum block does not need the true input signals and their complements at the same time.

2.3.2 Design of One bit Addition using LP Modulo 2 Addition and Equalizer Gates

The hybrid full adder that uses LP XNOR gates and output inverters is shown in Fig. 6. In order to achieve further power reduction, a new structure of a hybrid FA that combines branch-based logic and pass-transistor logic has been proposed and implemented [16].

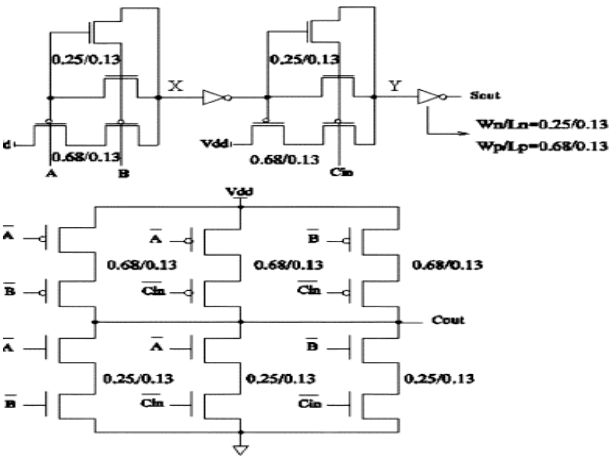

Fig. 6 – One bit addition with Driving Output

2.4 ULP FULL ADDER

The ULPD is obtained by the combination of an *n*-MOS and a *p*-MOS transistor, as shown in Fig. 7.

ULP leakage is obtained because when the ULPD is reverse biased, both transistors operate with negative voltages, leading to strongly reduced leakage current in comparison to standard diodes.

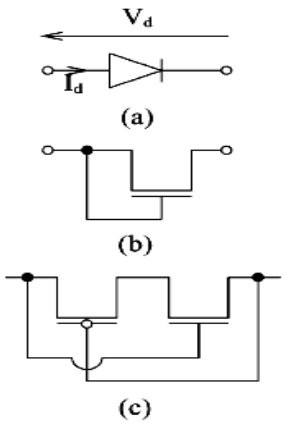

Fig. 7 – UPLD

The ULP full adder based on the LP equalizer gate and ULPD is shown in Fig.8 [16].

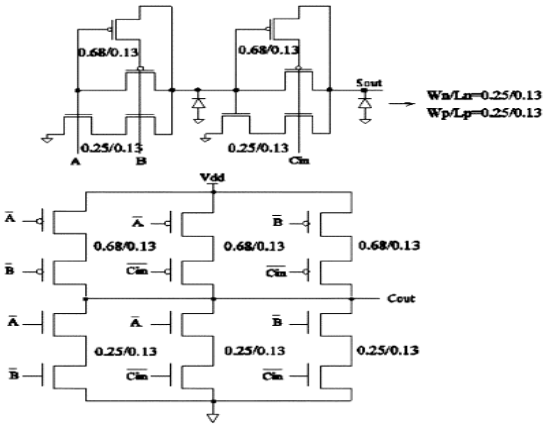

Fig. 8 – ULP Full Adder Using ULP Diodes

3. RESULTS AND DISCUSSIONS OF PROPOSED CNTFET ALU DESIGN

3.1 Proposed 8T Full Adder Using CNTFET

The basic building block of ALU is 8T CNTFET adder is shown in Fig. 10. The basic building block of adder is XOR gate is shown in Fig. 9. The XOR gate is implemented using only three transistors. The result it gives better footprint of the chip. If both the inputs are logically zero and one, then output is zero. Otherwise the output of XOR gate is logically one. The input pattern (0, 0) is applied to the circuit both M1, M2 and M3 transistors are said to be in cutoff region. When the input is $A = 0$ and $B = 1$, then the output is follows the input B, similarly the input is $A = 1$ and $B = 0$, then the output is follows the input A.

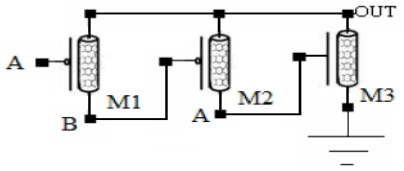

Fig. 9 – 3T XOR using CNTFET devices

The full adder is designed by using eight transistors and the corresponding equation are shown in (2), (3) and (4).

$$Sum = A \oplus B \oplus C_{in} \tag{2}$$

$$Carry = AB + BC + CA \tag{3}$$

$$Carry = (A \oplus B)C + AB \tag{4}$$

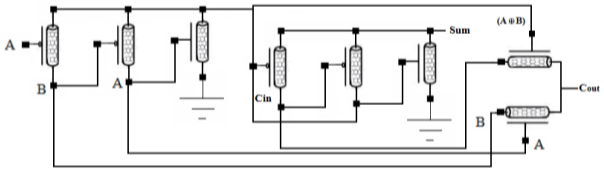

Fig. 10 – 8T 1 bit adder using CNTFET devices

Table 1 – Description of the proposed 1 bit adder using CNTFET

Design	Average Power (Watts)	Device Count
CMOS Full Adder	$4.948371 \cdot 10^{-4}$	28
CPL Full Adder	$8.388915 \cdot 10^{-4}$	32
HYBRID Full Adder	$5.412113 \cdot 10^{-4}$	24
ULP Full Adder	$1.862345 \cdot 10^{-4}$	24
CNTFET BASED HPLP Full Adder	$2.826373 \cdot 10^{-7}$	08

Table 1 shows the conventional full adder and proposed adder using CNTFET. The proposed adder results better power consumption than existing conventional techniques.

3.2 Proposed 2:1 and 4:1 Data Selectors Using CNTFET

A multiplexer (or mux) is a device that performs multiplexing; it selects one digital input signal and forwards the selected input into a single line. The CNTFET is also used for the designing multiplexers. Fig.11. and Fig. 12. Shows the schematic of 2:1 & 4:1 data selectors using CNTFET.

In table 2, power consumption of data selector using CNTFET was reported.

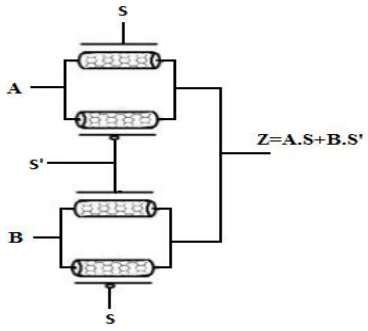

Fig. 11 – 2:1 Data Selector using CNTFET devices

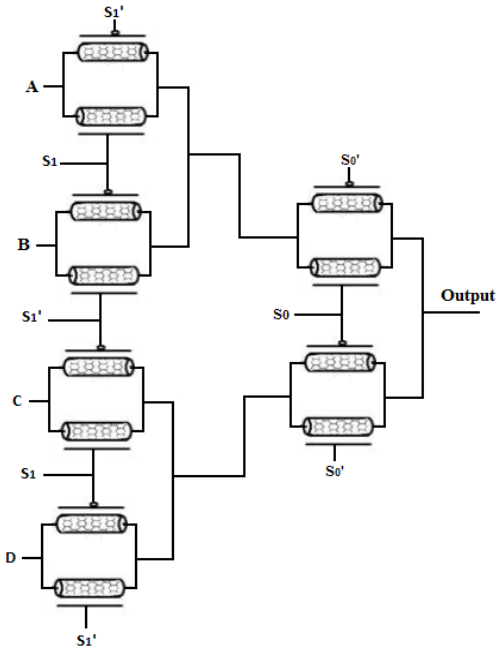

Fig. 12 – 4:1 Data Selector using CNTFET devices

Table 2 – Data selectors using CNTFET

Data Selector	MOSFET	**CNTFET**
2X1	6.583 μW	0.326 μW
4X1	7.742 μW	0.425 μW

3.3 PROPOSED ARITHMETIC AND LOGIC UNIT USING CNTFET ADDERS AND MULTIPLEXERS

The proposed ALU using CNTFET is shown in Fig. 13. For the INCREMENT and DECREMENT operations logic '1' and logic '0' are applied as inputs respectively. The complement of B is used for SUBTRACTION operation. The full adder performs the SUBTRACT operation by two's complement method. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation .From the simulation result is found that CNTFET based ALU is gives better results than conventional techniques and it is reported in Table 3.

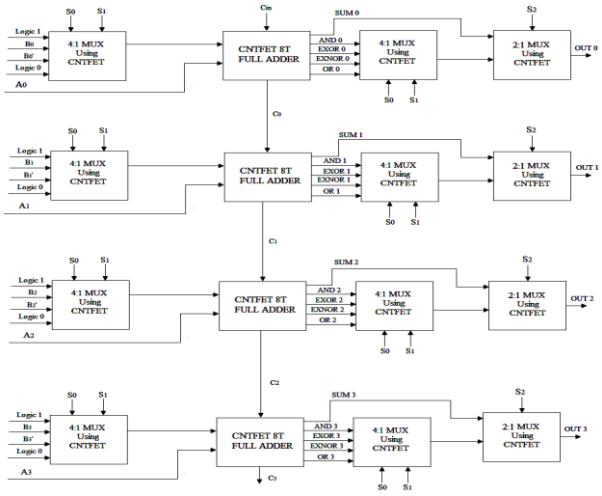

Fig. 13 – Proposed ALU using CNTFET

Table 3 – Proposed ALU using CNTFET

Existing ALU using conventional technique	$2.43 \cdot 10^{-2}$ Watts
Proposed ALU using CNTFET based 8T full adders and Multiplexers	$1.32 \cdot 10^{-1}$ Watts

4. CONCLUSIONS

In this the most suitable topologies of full adder cells static CMOS full adder, CPL full adder, Hybrid full adder, ULP full adder and CNTFET based low power high performance full adder were compared based on dynamic power and transistor counts in 45 nm technology. Simulation result has shown that the proposed CNTFET full adder and ALU significantly achieve better power and area reduction when compared with other commonly used full adders and ALU. An efficient and high performance DSP processor unit can be designed with the help of this proposed adder cell and ALU.

REFERENCES

1. S.K. Sinha, S. Chaudhury, *J. Electron Dev.* **2**, 1718 (2014).
2. S.S. Farahani, R. Zarhoun, M.H. Moaiyeri, K. Navi, *arXiv preprint arXiv:* 1303.2175 (2013).
3. M. Polimetla, R. Mahapatra, *World Academy Sci., Eng. Technol.* **60** No 5, 572 (2011).
4. G.B. Raja, M. Madheswaran, *Design and performance comparison of 6-T SRAM cell in 32nm CMOS, FinFET and CNTFET technologies* **70** No 21 (2013).
5. K.S. Saketh, P.R. Monica, *International Conference - In Advanced Electronic Systems (ICAES)*, 304 (2013).
6. S.K. Sinha, S. Chaudhury, *J. Semiconductors* **35** No 11, 114002 (2014).
7. S.L. Murotiya, A. Matta, A. Gupta, *Int. J. Electrical Electron. Eng.* **2** No 1, 78 (2012).
8. S. Cyril, D.K. Varugheese, *J. Theor. Appl. Inform. Technol.* **56** No **1**, 65 (2013).
9. M. Polimetla, R. Mahapatra, *World Academy Sci., Eng. Technol.* **60** No 5, 572 (2011).
10. S.A. Imam, N. Kalam, S. Abdhullah, *J. Nanosci. Nanotechno.* **14** No 3, 52 (2014).
11. M.H. Ben-Jamaa, K. Mohanram, G. De Micheli, *IEEE T. Computer-Aided Design of Integrated Circuits and Systems* **30** No 2, 242 (2011).
12. R.F. Mirzaee, T. Nikoubin, K. Navi, O. Hashemipour, *Microelectron. J.* **44** No 12, 1238 (2013).
13. S.S. Farahani, R. Zarhoun, M.H. Moaiyeri, K. Navi, *An efficient cntfet-based 7-input minority gate. arXiv preprint arXiv:* 1303.2175 (2013).
14. M. Moradi, R.F. Mirzaee, M.H. Moaiyeri, K. Navi, *16th CSI International Symposium In Computer Architecture and Digital Systems (CADS)*, 7 (2012).
15. S.K. Sinha, S. Chaudhury, *IEEE T. Nanotechnol.* **12** No 6, 958 (2013).
16. K. Nehru, A. Shanmugam. *Int. J. Comput. Appl. Technol.* **49** No 2, 134 (2014).