*JOURNAL OF NANO- AND ELECTRONIC PHYSICS*
Vol. **9** No 5, 05003(4pp) (2017)

*ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ*
Том **9** № 5, 05003(4cc) (2017)

# Simulation and Performance Analysis of 32 nm FinFet based 4-Bit Carry Look Adder

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(Received 16 June 2017; revised manuscript received 02 September 2017; published online 16 October 2017)

FinFET at 32 nm and beyond is an emerging transistor technology offer interesting delay–power tradeoff. FinFETs are a necessary step in the evolution of semiconductors because bulk CMOS has difficulties in scaling beyond 32 nm. Use of the back gate leads to very interesting design opportunities. Rich diversity of design styles, made possible by independent control of FinFET gates, can be used effectively to reduce total active power consumption IG/LP mode circuits provide an encouraging tradeoff between power and area. In the research work FinFET and MOSFET based adders are simulated as these devices are standout amongst the most generally actualized squares of microchip chips and advanced parts in the computerized incorporated circuit outline.

**Keywords:** FinFET, MOSFET, ADDER, 32 nm Technology, Power, Speed.

DOI: 10.21272/jnep.9(5).05003 PACS numbers: 75.40.Mg, 84.30.Sk, 85.40.Ls

## 1. INTRODUCTION

In past four decades CMOS scaling has offered improved performance from one technology node to the next. This in turn has brought smaller and faster digital systems. However, future bulk CMOS scaling faces considerable challenges due to material ad process technology limits [1]. According to the 2011 International Technology Roadmap for semiconductors (ITRS) [2], obstacles to the increased scaling of bulk CMOS include short-channel effects, sub-threshold leakage, gate-dielectric leakage, and device-to-device variations. These obstacles affect circuit and system reliability. The aforementioned challenges will become more prominent as CMOS scaling approaches atomic and quantum-mechanical physics boundaries [3]. Efforts to extend silicon scaling through innovations in materials and device structure continue.

FinFETs, which are double-gate field effect transistors, are able to overcome these scaling obstacles [2, 4]. One of the most important features of FinFETs is that the front and back gates may be made independent and biased to control the current and the device threshold voltage [5].

This ability to control threshold voltage variations offers a temporary means to manage the challenge of standby power dissipation. FinFET is considered a promising technology that can impact the immediate future due to its high-performance, low leakage power consumption, reduced susceptibility to process variations, and ease of manufacture using current processes [1]. Gate lengths of 10nm and below will be achievable with FinFETs. These features make FinFETs a strong candidate to bridge the technology gap between mainstream bulk CMOS and non-Silicon devices, such as carbon nanotubes.

FinFETs can be replacement for bulk-CMOS transistors in many different designs. Its low leakage/standby power property makes FinFETS a desirable option for adder circuits. Adder circuits are widely used in most digital and computer systems. The application of FinFET technology to adders can save significant power. Optimization can also be made to other modules, such a decoder and I/O buffers, to obtain power savings or a faster system.

Adder is one of the most vital components of a CPU (central processing unit), Arithmetic logic unit (ALU), and floating point unit and address generation like cache or memory access unit. On the other hand, increasing demand for portable equipments Such as cellular phones, personal digital assistant (PDA), and Notebook personal computer, arise the need of using area and Power efficient VLSI circuits. Low-power and high-speed adder cells are used in battery-operation based devices. As a result, design of a high-performance adder is very useful and vital [6].

The most well-known adders are the standard CMOS carry save adder, carry select adder and carry skip adder. In this paper, we present carry save adder, carry select adder and carry skip adder using CMOS and FinFET technology of 32 nm. The basic disadvantage of using CMOS technology is high average power dissipation and slow speed. These drawbacks were overcome in this paper by applying short gate FINFET technique to these adder designs.

There are the several types of FinFET which are Shorted-gate (SG) FinFET and independent gate (IG) [7-8] but here in this paper SG FinFET technique has been used. For SG FinFET, the two gates are connected together and direct replacement is served for conventional bulk-CMOS devices. Table 1 shows the advantages and disadvantages of FinFET based on design mode. For SG mode, the design performs fastest under all load conditions compare from another design mode. But the total of leakage is high. Opposite to the LP design mode, the total of leakage is very low and the switched capacitance also low. Unfortunately, this design has the slowest performance especially under load and area is overhead. The advantage for IG mode design, it performs low area and slow witched capacitance. But this design is unmatched pull-up and pull-down delays also experience high leakage. For IG/LP design mode, the advantages are low leakage, low switched capacitance and low area.

 

**Table 1** – Advantages and Disadvantages of FinFET [7]

| Design Mode | Advantage | Disadvantage |
|---|---|---|
| SG | Fastest under all load conditions | High leakage (1 μA) |
| LP | Very low leakage (85 nA) low switched capacitance | Slowest, especially under load. Area overhead routing |
| IG | Low area and switched capacitance | Unmatched pull-up and pull-down delays |
| IG/LP | Low leakage (337 nA), area and switched capacitance | Almost as slow as LP mode |

In this paper, simulation work is presented to compare the performance of CMOS and FinFet based carry look ahead, carry skip, and carry select adder circuit, with suitable power consumption and delay performance.

## 2. CARRY LOOK AHEAD ADDER

A carry-look ahead adder (CLAA) or fast adder is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits [9]. The logic circuit of CLAA is shown in Figure 1. For the implementation of CLAA, we require 14 transistor XOR circuits, 6 transistor AND circuits, 6 transistor OR circuits, 8 transistor AND circuits, 8 transistor OR circuits, 10 transistor OR circuits and 10 transistor AND circuits. The output waveform is shown in Fig. 2.

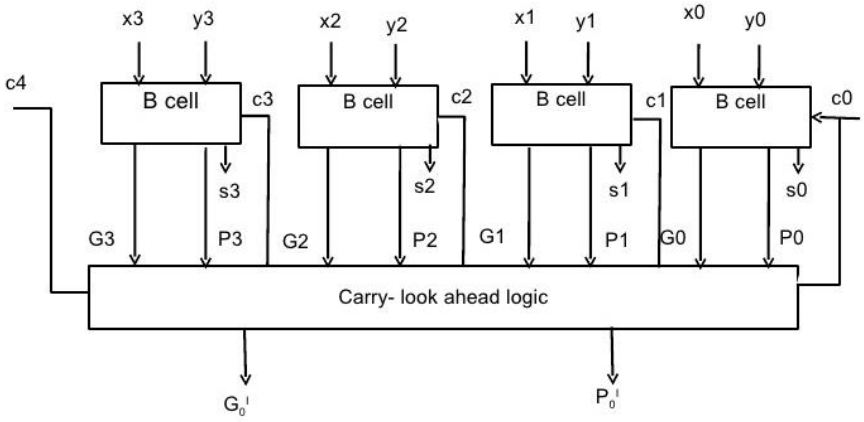


**Fig. 1** – Logic Circuit of Carry Look Ahead Adder.

## 3. CARRY LOOK AHEAD ADDER USING SHORT GATE FINFET

Short gate FinFET technique is applied on Carry Look Ahead adder. Here self-determining control Double Gate FINFET can be efficiently used to develop performance and reduce power consumption. In non-critical paths self-determining gate control can be used to join together parallel transistors. The operations of FINFET is recognized as short gate (SG) mode with transistor gates attached together, the independent gate (IG) mode where self-determining digital signals are used to drive the two device gates, the low power and optimum power mode where the back gate is attached to a reverse-bias voltage to reduce leakage power and the hybrid mode, which employs a arrangement of low power and self-determining gate modes.

In due to its base material the uninterrupted down in scaling of bulk CMOS creates key issues. The crucial obstacles to the scaling of bulk CMOS to 45 nm gate lengths include short channel effects, optimum current, gate-dielectric leakage, and device to device variations. But FINFET based designs offers the superior control over short channel effects, low leakage and better yield [10] in 45 nm helps to overcome the obstacles in scaling. The operating voltage waveform of Carry Look Ahead Adder using DG FINFET technique is shown in Fig. 2. The output input and output voltages with timing sequence are tabulated in Table 2 for CMOS and DG FINFET carry look ahead adder.

As we can see from above two figures, there is no change in the waveforms. Digital CMOS circuit may have three major sources of power dissipation namely dynamic, short and leakage power. Hence the total power consumed by every MUX style can be evaluated using the equation 1.

$$P_{tot} = P_{dyn} + P_{sc} + P_{leak} \quad (1)$$

$$P_{tot} = CLV_{dd}Vf_{clk} + I_{SC}V_{dd} + I_{leak}V_{dd} \quad (2)$$

Thus for low-power design the important task is to minimize $CLV_{dd}Vf_{clk}$ while retaining required functionality. The first term $P_{dyn}$ represents the switching component of power, the next component $P_{sc}$ is the short circuit power and $P_{leak}$ is the leakage power. Where, $CL$ is the loading capacitance, $f_{Clk}$ is the clock frequency which is actually the probability of logic 0 to 1 transition occurs (the activity factor). $V_{dd}$ is the

| Timing Sequence | CMOS Input and Output (1V) | | | | | | |
|---|---|---|---|---|---|---|---|
| | Input $A_0$ | Input $B_0$ | Output $C_0$ | Input $A_1$ | Input $B_1$ | Output $S_1$ | Output $C_1$ |
| **TON (nsec)** | 0 to 50 | 0 to100 | 0 to 80 | 0 to 50 | 0 to 100 | 2 to 55 | 1 to 82 |
| **TOFF (nsec)** | 0 to 50 | 100 to 200 | 80 to 100 | 0 to 50 | 100 to 200 | 55 to 82 | 82 to 105 |
| **DG FINFET Input and Output (1V)** | | | | | | | |
| | Input $A_0$ | Input $B_0$ | Output $C_0$ | Input $A_1$ | Input $B_1$ | Output $S_1$ | Output $C_1$ |
| **TON (nsec)** | 0 to 50 | 0 to100 | 0 to 80 | 0 to 50 | 0 to 100 | 0 to 50 | 0 to 80 |
| **TOFF (nsec)** | 0 to 50 | 100 to 200 | 80 to 100 | 0 to 50 | 100 to 200 | 50 to 80 | 80 to 100 |

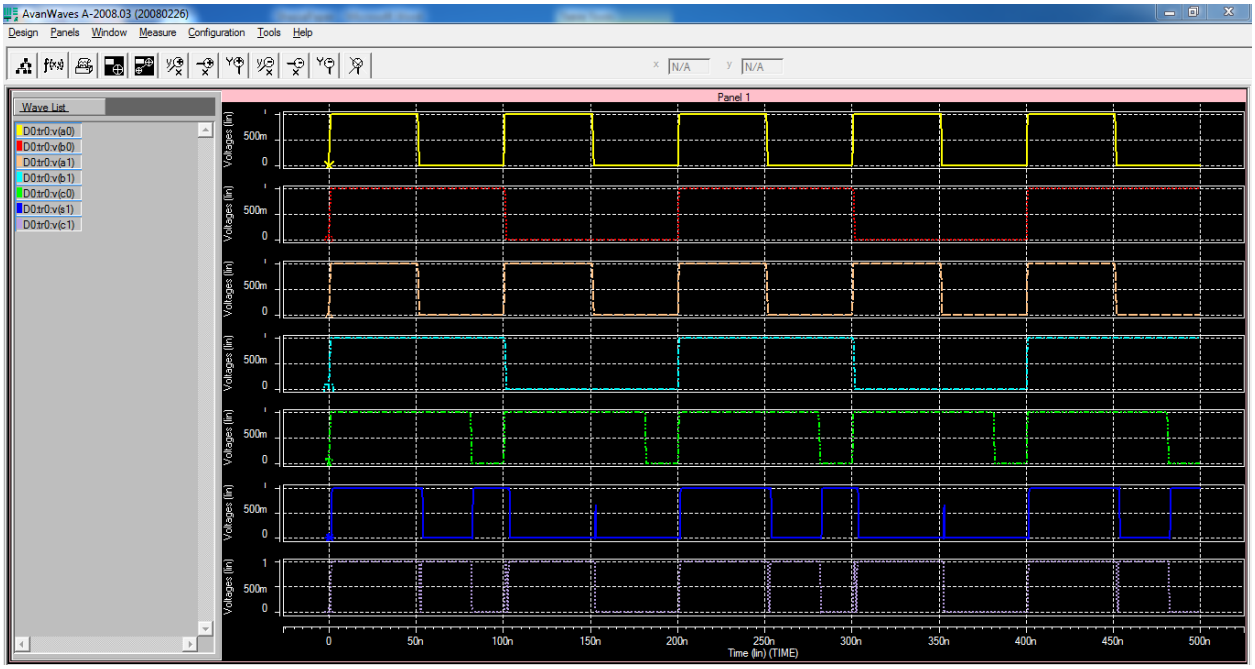


**Fig. 2** – Timing sequence of 32 nm FinFet Carry Look Ahead Adder

**Table 2** – MOSFET dimension specification.

| | W | L | AS | PS | AD | PD |
|---|---|---|---|---|---|---|
| **P- MOS** | 100 nm | 32 nm | 2.25 pm | 6.8 µ | 2.25 pm | 6.8 µ |
| **N-MOS** | 64 nm | 32 nm | 2.25 pm | 6.8 µ | 2.25 pm | 6.8 µ |

**Table 3** – FINFET dimension specification.

| | TFIN | Lf | NFIN | NRS | NRD | HFIN |
|---|---|---|---|---|---|---|
| **P- MOS** | 2 nm | 32 nm | 1 | 1 | 1 | 2 nm |
| **N-MOS** | 2 nm | 32 nm | 1 | 1 | 1 | 2 nm |

supply voltage, V is the output voltage swing which is equal to $V_{dd}$; but, in some logic circuits the voltage swing on some internal nodes may be slightly less [11].

The current Isc in the second term is due to the direct path short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground [12]. Finally, leakage current Ileak, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

## 4. SIMULATION RESUTS AND DISCUSSION

A Carry Look Ahead Adder based on DG FINFET technique has been proposed. The specifications of 32 nm MOSFET and FinFET are as shown in Table 3 and 4 respectively. Where the parameters are

W = Channel Width
L = Channel Length
AS = Source Diffusion Area
AD = Drain Diffusion Area
PS = Perimeter of the source junction, including the channel edge
PD = Perimeter of the drain junction, including the channel edge
TFIN = Fin-thickness
Lf = Gate length
NFIN = Number of Fins
NRS = Squares of Source Diffusion
NRD = Squares of Drain Diffusion
HFIN = Fin height

The analysis of the simulated results confirms the feasibility of the DGFINFET technique in carry look ahead adder design and shows that there is reduction in the value of power dissipation parameter and delay as compared to CMOS technique at supply voltage of 1V.DG FINFET adders have a marginal increase in area compared to the CMOS adders; overall, we achieved the lowest power dissipation. Simulation result is measured by CANDENCE VIRTUOSO Tool. The simulation result is summarized in Table 4.

**Table 4** – Power and delay parameters.

| Parameters | CLAA MOSFET | CLAA FinFET |
|---|---|---|
| Supply Voltage | 1V | 1V |
| Technology (nm) | 32 | 32 |
| Average Power Dissipation (μW) | 146.77 | 2.92 |
| Delay(nS) | 1.14 | 0.12 |

From the above table, it is clear that the performance of carry look ahead adder using FinFET has been improved. It is shown more clearly with the help of chart in Fig. 3.

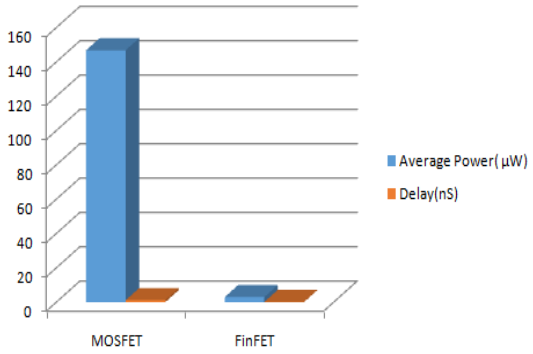


**Fig. 3** – Carry Look Ahead Adder power and delay rating.

We have experimentally investigated the device performance and parameters such as operating current, average power dissipation and delay of Carry Look Ahead Adder using FINFETs with the help of cadence virtuoso at 32 nm technology. It is clear that the average power dissipation and delay in Carry Look Ahead Adder is reduced drastically by using FinFET.

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