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An Analytical Modeling of Drain Current for Single Material Surrounded Gate Nanoscale SOI MOSFET

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In this paper, we have presented modeling of drain current for single material surrounded gate SOI MOSFET (SMG SGT SOI MOSFET) whose channel length is 40nm. We have studied the behavior of device by varying various device parameters in Linear, Saturation, and Sub-threshold regions. We have also presented a drain current model incorporating DIBL. The comparison between previously presented model with channel length = 50 nm and our scaled model is also presented in various regions of device operation.

Keywords: SMG SGT SOI MOSFET, Linear region, Sub-threshold, Saturation, DIBL

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1. INTRODUCTION

Reducing down or scaling down of traditional MOSFET has been of main focus. Reducing the device dimensions improves performance of device and it leads to less power consumption. Scaling is the most outstanding technological challenge in today's era [1, 2]. Devices used for the nano scale applications are based on many gate structures like – two Gate or double gate (DG) [3], three gate or triple gate [4, 5] or fin shaped gate (FinFET) [6, 7] and gate all around(GAA) or cylindrical gate/or surrounded gate (CGT/SGT) [8, 9]. These devices can be regarded as near ideal technology, and can be used for manufacturing IC's. They offer many advantages than single gate SOI MOSFET such as higher drive current, high package densities, low sub threshold slope. The main reason of these advantages is – the better control over the channel region. And due to this, these structures are strongly immune to short channel effects (SCE's) [10].

We know that when we reduce the dimensions of channel region below a particular value, it leads to many short channel effects (SCEs). Charge sharing also reduces the ability of the gate voltage to control the drain current. The surround gate SOI MOSFET [11-13] is a solution (actually one of the solutions) for improving the device performance and also for controlling limitations due to scaling. In surrounded gate SOI MOSFET, the gate surrounds the channel from all sides. Gate in surrounded gate SOI MOSFET is of cylindrical form and the drain and source regions lie on the two edges of the MOSFET. Due to the gate surrounding the channel from all the sides, there is better control over the channel region, SCEs are reduced and the performance of device is improved. Dual material surrounded gate MOSFET (SGT MOSFET) is also a solution for better performance and reduced short channel effects (SCEs). The only problem in dual material surrounded gate MOSFET (DMG SGT MOSFET) is it's complex manufacturing process and structure, which leads to complex calculations. Single material surrounded gate MOSFET (SGT MOSFET) is simple to manufacture as compared to the dual material SGT MOSFET.Single material surrounded gate SOI MOSFET can be shown in the Fig. 1.

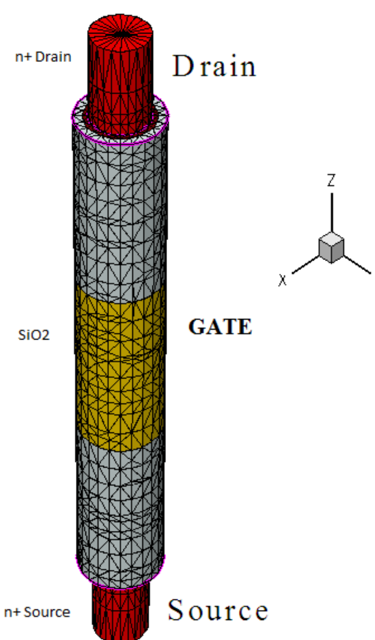

Fig. 1 – Surrounded gate SOI MOSFET

In this work, we have developed a complete drain current model. The effectiveness of the nano scaled single material surrounded gate SOI MOSFET has also been compared with performance of dual material surrounded gate MOSFET of channel length 50 nm.

2. ANALYTICAL MODELING

Different regions of operation are discussed below:

2.1 Linear Region

In order to obtain the drain current model, first drain currents are obtained in source and drain ends and then, an expression is obtained for linear region. The drain current in the strong inversion region is mainly given by drift tendency and we can express it as [14]:

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$$I_{ds}(z) = 2\pi R Q_n(z) \frac{\mu(dV(z)/dz)}{1+(1/E_{sat})(dV(z)/dz)}, \quad (1)$$

where $2\pi R$ device width, R is the radius. $V(z)$ – potential of channel along z direction. $dV(z)/dz$ is the electric field along z direction. E_{sat} is critical electric field and is equal to $2V_{sat}/\mu$. V_{sat} is simply the Saturation velocity. μ – mobility, and is given as:

$$\mu = \frac{\mu_0}{\sqrt{(1+[N_A/(N_{ref}+(N_A/S))])}}, \quad (2)$$

where μ_0 – electron mobility with value 677 cm^2/V$_s$.
N_{ref} and S involve tradeoffs between impurity scattering and photon, respectively and are given as $N_{ref} = 3\cdot 10^{22}$ m^{-3}, $S = 350$. N_A – doping concentration of p type region. $Q_n(z)$ is the surface charge density at point z and is given by:

$$Q_n(z) = C_{ox}(V_{gs} - V_{th} - V(z)), \quad (3)$$

where, V_{gs} is the gate to source voltage. V_{th} is the threshold voltage. And C_{ox} – gate oxide capacitance per unit area of SMG SGT MOSFET and is given as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad (4)$$

where

$$\varepsilon_{ox} = \varepsilon_0 \varepsilon \quad (5)$$

Now, in order to obtain the complete drain current equation for linear region, equation (1) is simplified. Substituting equations (2) to (5) in equation (1), and integrating, following drain current equation for linear region is obtained:

$$I_{ds} = \frac{2\pi R \mu C_{ox}(V_{gs} - V_{th} - \frac{V_{dt}}{z})}{L(\frac{1}{V_{ds}} + \frac{1}{LE})}, \quad (6)$$

where, V_{ds} – drain to source voltage

$$E = 2V_{sat}/\mu \quad (7)$$

2.2 Saturation Region

In this region, drain current equation is expressed as [14]:

$$I_{dsat} = 2\pi R V_{sat} Q_{nsat} \quad (8)$$

where, I_{dsat} – represents saturation drain current, and Q_{nsat} – inversion charge obtained at $V_{ds} = V_{dsat}$ and is given by:

$$Q_{nsat} = C_{ox}(V_{gs} - V_{th} - V_{dsat}) \quad (9)$$

Using above equation in eq. (8), we get

$$I_{dsat} = 2\pi R V_{sat} C_{ox}\left(V_{gs} - V_{th} - V_{dsat}\right) \quad (10)$$

where, V_{th} is threshold voltage of SMG SGT MOSFET. V_{dsat} is the drain saturation voltage and can be obtained by equating Eqs. (6) And (10) at $V_{ds} = V_{dsat}$ and is given as:

$$V_{dsat} = \frac{V_{gs} - V_{th}}{1 + (V_{gs} - V_{th})/LE} \quad (11)$$

As the length of the channel of the device reduces, short channel effects (SCEs) like drain induced barrier lowering (DIBL) comes into action and it affects the behavior of the device. Due to DIBL, the charge in channel in short channeled devices is mainly controlled by the drain potential instead of being controlled by gate potential which causes threshold voltage to roll off and degrades the performance of our device. So, it is important that we incorporate DIBL effect in our SMG structure so that we can develop precise model of the drain current. DIBL can be defined as [14]:

$$DIBL = V_{th}(V_{ds} = 0.05) - V_{th}(V_{ds}) = V_{th_lin} - V_{th_sat}, \quad (12)$$

where, V_{th_lin} – Threshold voltage in linear region. V_{th_sat} – Threshold voltage in saturation region.
We can incorporate DIBL effect in the above model of drain current by replacing threshold voltage (V_{th}) in Eq. (6) by V_{th}"

$$V_{th}^{"} = V_{th} \cdot DIBL \quad (13)$$

Using Eqs. (11) And (12), we can write

$$I_{ds(DIBL)} = \frac{2\pi R \mu C_{ox}[V_{gs} - V_{th}^{"} - \frac{V_{dt}}{z}]}{L(\frac{1}{V_{dt}} + \frac{1}{LE})} \quad (14)$$

Now, when V_{ds} is higher than V_{dsat}, the pinch off point or the saturation velocity moves towards source and difference in the voltage ($V_{ds} - V_{dsat}$) is dropped along the length l_d. It results in smaller channel length than physical channel length and it induces an increase in drain current.

The drop in velocity at the velocity saturation region is given by [14]

$$V_{ds} = V_{dsat} + I_{sat} E \sinh(l_d/l_{sat}) \quad (15)$$

where, l_d – length of velocity saturated region, and l_{sat} – characteristic length of the velocity saturated region and is considered as the fitting parameter.

Hence, with CLM effect included, we can obtain the saturation current simply by replacing the term L by L-l_d in Eq. (14) and can be expressed as:

$$I_{dsat} = \frac{2\pi R \mu C_{ox}[V_{gs} - V_{th} - \frac{V_{dsat}}{z}]}{\frac{L - l_d}{V_{dsat}}(1 + \frac{V_{ds}}{(L - l_d)E})} \quad (16)$$

Table 1 – Parameters and their values used in simulation

Parameters Used	Values
Boltzmann constant (k)	1.3807×10^{-23} JK^{-1}
Permittivity of free space(ε_0)	8.85×10^{-12} F/m
Elementary charge(q)	1.6×10^{-19} C
Thermal Voltage(V_T)	0.0258V
Temperature(T)	300K
Carrier conc. of Si (Intrin sic) (n_i)	1.45×10^{16} m^{-3}
Carrier conc. (Conduction band) (N_c)	2.8×10^{25} m^{-3}
Carrier conc. (Valence band) (N_v)	1.04×10^{25} m^{-3}
Saturation velocity(V_{sat})	10^5 m/s

2.3 Sub-threshold Region

This current is leakage current which affects dynamic circuits and determines the standby power consumption in Very Large Scale Integration (VLSI). This regime describes switching behavior of devices and is very important for the low power applications. So, it is important to maintain quite good sub-threshold characteristics. This current can be obtained using the min. surface potential and can be expressed as:

$$I_{sat}=[\frac{2\pi R\mu C_{ox}}{L}V_t^2(\exp\{\frac{V_{gs}-V_{th}}{2V_t}\})(1-\exp(\frac{-V_{gt}}{V_t})] \quad (17)$$

where, V_t – thermal voltage and is given by:

$$V_t=\frac{kT}{q} \quad (18)$$

3. RESULTS AND DISCUSSIONS

In order to analyze the importance of silicon-single material SGT SOI MOSFET design, we modeled various parameters and we then compared our results obtained for scaled SMG with DMG.

The proposed model of drain current is accomplished for channel length equal to, $L = 40$ nm, radius of the device, $R = 15$nm, oxide thickness equal to, $t_{ox} = 3$ nm, uniformly doped Source and/or drain, N_D having doping density approx 5×10^{19} cm^{-3}, p substrate doping, N_A having doping density 10^{16} cm^{-3}. We have used Drift diffusion model [9] and we have neglected quantum mechanical effect [15]. Various constants and other parameters which were used in the analysis and/or simulation are shown in Table 1.

Fig. 2 shows variation of drain current as a function of drain to source voltage in linear region of device operation at $V_{gs} = 1.6$ V, $V_{gs} = 1.8$ V and $V_{gs} = 2$ V, V_{ds} is varied from 0 V to 1 V and $V_{th} = 0.3$ V. Drain current is calculated in Amperes. The linear behavior can be seen from the graph for V_{ds} almost up to 0.1 V.

Fig. 3 shows the comparison between the nano scaled device whose parameters were stated above with non scaled DMG device having parameters: channel length equal to, $L = 50$ nm, radius of the device is, $R = 10$ nm, oxide thickness is equal to, $t_{ox} = 2.5$ nm, uniformly doped Source and/or drain, N_D having doping density 5×10^{19} cm^{-3} p substrate doping, $_A$ having doping density 10^{16} cm^{-3}, work-function at the Nsource end (Ø_{m1}) is equal to 4.8 eV (Au) and work- function at the drain end (Ø_{m2}) is equal to 4.4 eV (Ti).

It can be clearly seen from Fig.3 that the nano scaled SMG leads to increase in drain current in comparison to DMG device. So, that means that the performance of the SMG device is better than the DMG of channel length 50 nm.

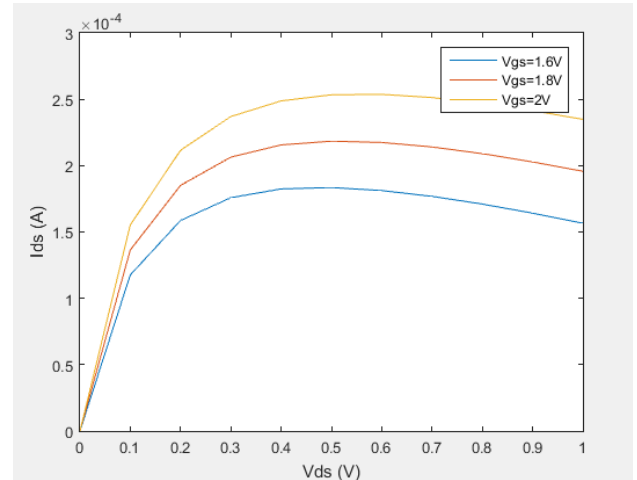

Fig. 2 – Variation of I_D as a function of V_{DS} at different gate bias in linear region of device Operation

Above comparison was in the linear region of device operation. Now, we will encounter the performance of our device in the Saturation region.

Fig. 4 Shows the variation of drain current (I_D) as a function of drain to source voltage (V_{DS}) at $V_{gs} = 1.9$ V, $V_{gs} = 2.9$ V, and $V_{gs} = 3.9$ V, and V_{ds} is varied from 0 V to 1.4 V and, $V_{th} = 0.3$ V. Saturation occurs somewhere near $V_{ds} > 0.4$ V. It can be seen from the graph that Saturation behavior is more prominent at higher values of V_{gs}. As V_{gs} is increased, saturation curve becomes straighter.

We also compared the behavior of our device with the DMG and analyzed the results. Fig. 5 shows the comparison of drain currents between SMG and DMG at same V_{th} and different values of V_{gs}.

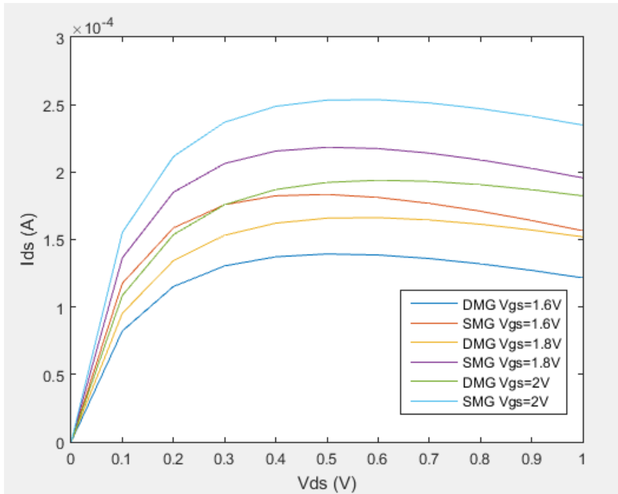

Fig. 3 – Comparison of drain currents in nano Scaled SMG and DMG (L = 50 nm) at different V_{gs} in linear region

As seen from the graph, it is evident that the nano scaled SMG exhibit better performance than DMG. The current value is higher in SMG than in DMG which means that in SMG a small voltage can cause higher current to flow as compared to the DMG in which at the same voltage less current will flow than SMG.

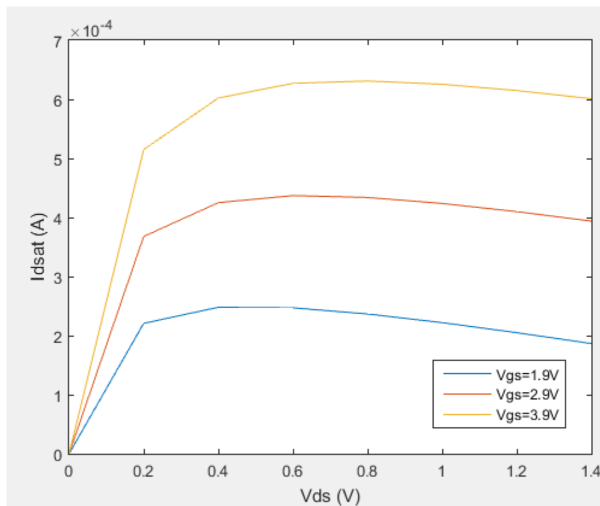

Fig. 4 – Variation of I_D with respect to V_{DS} at different gate bias in Saturation region of device operation

Now, for the Sub-threshold region, we calculated the sub threshold current at various values of drain to source bias with V_{th} = 0.3 V and at three values of gate to source potential: V_{gs} = 0.20 V, V_{gs} = 0.24 V, and V_{gs} = 0.26 V. Fig. 6 shows the drain current variation with respect to drain to source voltage for the sub threshold region. Drain to source (V_{ds}) in the graph is varied from 0 V to 0.05 V with a very small varying interval of 0.02 V. It can be clearly seen that the value of sub threshold current is very small which suggests

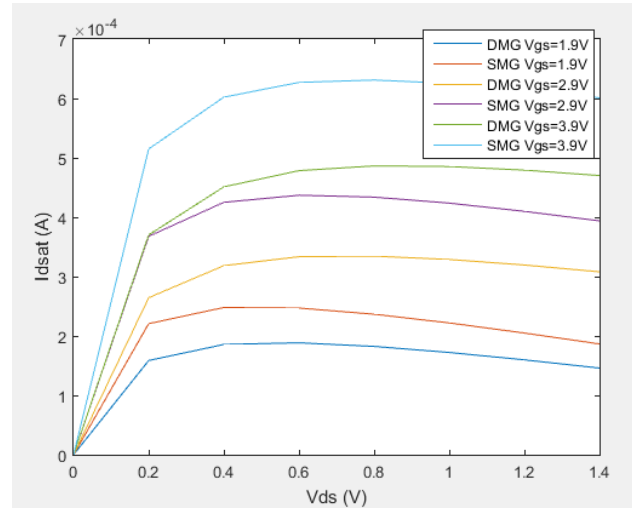

Fig. 5 – Comparison of drain currents in nano Scaled SMG and DMG at different V_{gs} in Saturation region

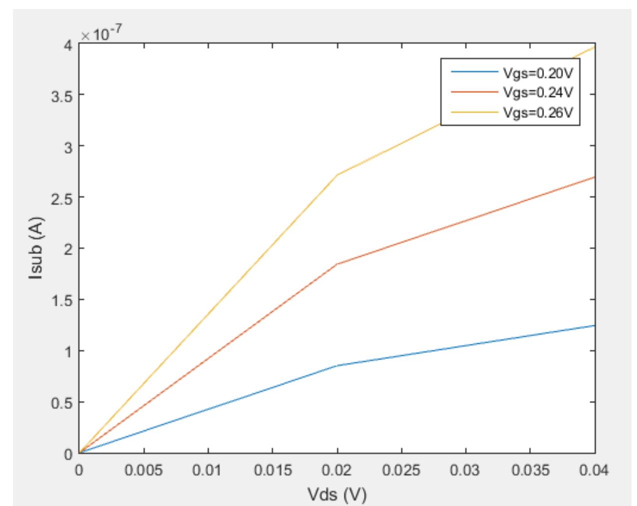

Fig. 6 – Sub threshold or leakage current at different gate to source bias

that during switching, leakage current with be very minute in our nano scaled device.

4. CONCLUSIOS

A single material surrounded gate SOI MOSFET structure is presented as well as analyzed. We developed a complete efficient model of drain current to anticipate the current-voltage characteristics. Further, the drain current model of the nano scaled Single material Surrounded gate SOI MOSFET was compared with Dual material surrounded gate MOSFET structure with channel length 50 nm. It has been manifested that SMG design is not only simpler but it also offers quite superior characteristics in terms of higher drain current.

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