Journal of Nano- and Electronic Physics
Vol. **11** No 5, 05019(5pp) (2019)

Журнал нано- та електронної фізики
Том **11** № 5, 05019(5cc) (2019)

Impact of Defects on Quality Contact Systems for Photoelectric Converters

O.Y. Nebesniuk*, Z.A. Nikonova, A.A. Nikonova, S.L. Khrypko

Engineering Institute of Zaporizhzhya National University, 226, Soborny Ave., 69006 Zaporizhzhya, Ukraine

(Received 27 April 2019; revised manuscript received 20 October 2019; published online 25 October 2019)

Energy is a main factor and it stays at the center of economic, social and ecological tasks of modern development. The article suggests directions for improving the quality of traditional as well as the development of new semiconductor materials and different types of metallization. The use of epitaxial compositions for the production of photoelectric converters promises particularly great prospects. The tendencies of creation of the most complex electronic devices on the basis of multilayer epitaxial structures are clearly shown. At the same time, very high requirements are imposed on the electrophysical properties and perfection of the structure of each layer; the problems of creating perfect and sharp *p-n* junctions and heteroboundaries on large areas of epitaxial compositions are posed.

Keywords: Plate, Defects, Epitaxial compositions, Contact systems, Photoelectric converters.

DOI: 10.21272/jnep.11(5).05019 PACS numbers: 85.40.Ls, 85.40.Ry

1. INTRODUCTION

Nowadays solar energy is one of the most promising ways of eco-friendly source of electricity. The main task of the solar energy use is to reduce its price to minimum or even to zero. As we know, photovoltaic method of conversing solar energy is of the greatest interest among methods, which are used in non-traditional energy. The technology of photoelectric converters (PC) creation includes production of plates and source components, contact systems and voltage removing nets for them, distribution of received samples for separate elements and others.

The main benefits of silicon PC are high steady efficiency (productivity is about 20 %); technology of silicon epitaxial layers does not require further quick thermal burn; rather low cost of electricity which is generated by them; opportunity for production on different silicon plates; technology does not require the use of rate elements; the absence of toxic elements that is very important regarding to the problem of their recycling which serves their term.

Nowadays, the rate of useful effect of silicon PC is about 15-20 % (polycrystals-monocrystals). Existing laboratory samples of monocrystalline centers show 25 % productivity and of polycrystalline centers – 20.5 %. Theoretical efficiency of silicon single-junction elements is 33.7 %.

However, this has not yet been achieved, and the main task, apart from increasing the efficiency of the cells, is to improve the production technology of cheaper photovoltaic modules. Such modules on thin films are produced using the method of deposition of amorphous hydrogenated silicon in a glow discharge plasma of the hushed discharge and advanced postgrowth technologies.

It is known that photovoltaic modules consist of two monolithic interconnected transitions in amorphous and nanocrystalline silicon. The introduction of the nanocrystalline transition, which has significant light absorption in the near infrared region, allows to extend the light absorption band and, in turn, increase the efficiency of PC. Another advantage is the possibility of reducing the thickness of amorphous transition, unstable relative to intense light, which reduces the degradation of the module.

Today the company "Oerlikon Solar" offers the most advanced technology for the production of photovoltaic modules, which is confirmed by two international awards, the awarded this technology ("Thin Film Innovation Award 2009", "Cell Award 2009"). Equipment company, "Oerlikon Solar" is intended for the manufacture of plates of 1.1×1.3 m^2 (module 1.43 m^2). The choice of this size allows to optimally combine high performance hardware with convenience in transportation and installation of the photoelectric module.

Separately, it should be noted the PC of "Sanyo". They are produced according to HIT (Heterojunction wit Intrinsic Thin layer) with the use of several silicon layers similarly to tandem multilayer cells. Efficiency of such elements from monocrystalline C-Si and several layers of nanocrystalline nc-Si is 23 % [1]. Nowadays it is the highest efficiency of serial PC. There are three basic types of non-organic film solar elements: silicon films based on the amorphous silicon (a-Si), films based on cadmium telluride (CdTe) and films based on selenide midi-indium and helium ($CuInGaSe_2$, or CIGS).

Efficiency of modern thin-film solar batteries based on the amorphous silicon is 10-11 % (produced by First Solar Company), based on selenide midi-indium and helium is 12-13 % (Japanese solar modules SOLAR FRONTIER), efficiency of separate thin-film solar batteries is higher. For example, the figures on laboratory samples productivity of amorphous silicon elements are 12.2 % (Unites Solar Company), of CIGS elements are 20.5 %. So far, solar converters based on thin films of amorphous silicon are leading in production volumes among other thin-film technologies. The global market for Si thin-film elements is about 80 %, and solar cells based on cadmium telluride are about 18 % of market. First of all it is connected with the price and availability of raw material and with higher characteristic stability. We note that silicon, one of the most widespread elements in the Earth's crust, Indium (CIGS elements)

*0811oksana@gmail.com

and telluride (CdTe elements) are diffuse and obtained in small quantities. Besides, cadmium (CdTe elements) is toxic though the most producers of such solar panels guarantee the full recycling of their product. Fraunhofer institute that learns solar energy systems, Soitec, CEA-Leti and Berlin Helmoltz center announced that they reached a new world record of converting solar energy into electricity, they used a new structure of solar elements with four layers as some other multilayer photo elements. This micro-scheme is used for work with a hub, which concentrates sunlight by 297.3 times that is the area of the hub's lens is about 300 times bigger than photo element area. Efficiency of 44.7 % refers to a wide range of solar radiation: from ultraviolet to infrared. Four layers of the center take away energy waves with the length 200-1800 nm.

These solar elements are used in photoelectric hub, its technology, productivity for converting sun light into electricity. With such connection between solar elements, the cells made of semiconductors III-V are put over each other. Each layer absorbs the waves of different length solar spectrum.

2. DESCRIPTION OF THE OBJECT AND METHODS OF RESEARCH

In modern production of semiconductor supplies and integrated circuits, silicon one-layer epitaxial structures (SOES) and silicon structures with dielectric isolation (SSDI) are widely used. The actual task is a careful examination of the defects on different technological stages of PC production.

The goal is to learn the defects of SOES and to develop a system that has a higher resistance to electromigration and at the same time prevents silicon erosion in contact boxes.

The analysis shows that the most substantial source of defect sib epitaxial structures is voltage that appears in them during crystallization of further cooling from production temperature. The main reasons of voltage appearance are the following: the difference between lattice periods of materials that are accompanied by $\Delta\alpha$, which leads to the voltage inconsistency $\sigma_{\Delta\alpha}$; the difference $\Delta\lambda$ between the indices of thermal expansion of materials or unequal temperature distribution along the thickness and surface of increased layer, that is a source of thermal voltage in epitaxial composition; the presence of the composition gradient according to thickness of epitaxial layer; increased concentration of structure defects on the interfaces.

In very thin films, the powers of surface tension on extra voltage source, according to the notice of surface energy, can lead to the clenching or stretching of increased layer. The resulting stress, depending on their magnitude, the plasticity of the material of the epitaxial structure, the thickness of the growing layers, and the thermal conditions of the treatment, may partially change with the formation of dislocations. Residual stress causes elastic deformation of epitaxial structures.

Inconsistency voltage is determined with inconsistency of lattice period f [1]:

$$\sigma_{\Delta\alpha} = \frac{E}{1-\nu} f ,$$

$$f = \frac{\Delta\alpha}{\alpha}, \quad (1)$$

where E is the elasticity unit, ν is the Poison index, $\Delta\alpha = \alpha_p - \alpha_l$ is the difference between periods of lattice plate and a layer, that they increase, $\bar{\alpha}$ is the average value of material lattice period.

The index of voltage disparity depending on indexes Δa differs within wide limits. The minimum is in a homoepitaxy where disparity index of lattice periods is not more than $f \le (2 \div 4) \cdot 10^{-4}$. Within heteroepitaxy, f can represent units of percent, and relevant voltage disparity counted in flexible approach can even exceed the material.

As the voltage disparity appears in the process of epitaxial layer increase under crystallization temperature, it means the maximum temperature in the system; there is a good chance of their relaxation in the very sludge progress causing disparity dislocations and other defects.

It is established that the thermal stresses in the epitaxial structures can be caused both by the difference in the coefficients of thermal expansion of the materials and by the uneven distribution of temperature within the layer. In the first case, the thermal stress due to the difference in the coefficients of thermal expansion of the substrate and the layer of build-up occurs in the process of heat treatment of the epitaxial structure. Their value and sing are determined by the difference between changes of lattice plate periods and the film under increasing temperatures and are calculated:

$$\sigma_{\Delta\lambda} = \frac{E}{(1-\nu)\left(\frac{\lambda_p^T - \lambda_p^{T_0}}{\bar{\lambda}_p} - \frac{\lambda_l^T - \lambda_l^{T_0}}{\bar{\lambda}_l}\right)}, \quad (2)$$

where λ_p^T, λ_l^T are the lattice plate and epitaxial layer periods under increasing temperature; $\lambda_p^{T_0}, \lambda_l^{T_0}$ are the same periods under measuring temperature; $\bar{\lambda}_p, \bar{\lambda}_l$ are average indexes of lattice plate and layer periods within the temperature range that is analyzed.

The second equation was voltage on the interface if there is no plastic deformation relationship with the famous term for thermal voltage calculation:

$$\sigma_{\Delta\lambda} = \frac{E}{1-\nu} \Delta\lambda \Delta T , \quad (3)$$

where $\Delta\lambda$ is the difference between temperature indexes of the plate (which increases) and epitaxial layer in the analyzed temperature period.

Thus, $\sigma_{\Delta\alpha}$, depending on their magnitude, as well as the mechanical properties of the material and growing conditions, can lead to elastic, plastic deformation or mechanical failure. It should also be noted that, depending on the difference between $\Delta\alpha$ and $\Delta\lambda$, the substrate and the voltage layer can both consist of $\sigma_{\Delta\lambda}$ and compensate it. Because of the little index of $\Delta\lambda$ ($\sim 10^{-6}\,\mathrm{K}^{-1}$), $\sigma_{\Delta\lambda}$ is usually less than $\sigma_{\Delta\alpha}$, and the main reason of dislocations appearing is the difference be-

tween lattices periods.

For the investigation, dislocation-tree silicon plates are widely used as linings in production of silicon epitaxial compositions. It is determined that in the process of epitaxy besides thermal voltage, voltages from this action are much stronger with epitaxial layer increase 300-500 μm long. In conditions of quite long (0.2-3.0 hours) process of appearing voltage and high temperatures (1400-1500 K), defect formation in the increasing film and in the composition lining takes place; structure deficiencies of the primary lining have a great impact on their development [2].

3. DESCRIPTION AND ANALYSIS OF THE RESULTS

Investigations took place on the linings for SOES made of dislocation-tree monocrystalline silicon, alloyed with the antimony for the resistance 10^{-4} Ohm·cm; and linings of the silicon epitaxial structures are made of non-alloyed dislocations with the monocrystals of hole conductivity with the resistance 60-100 Ohm·m. The linings completed standard cycle of mechanical treatment that includes monocrystal's cutting using a skive with inner cutting edge on the plates 380 μm long with 28, 40 or 60 mm diameter and 500 μm long with 76 mm diameter, polishing with diamond compounds and chemo-mechanical polishing with suspension based on aluminosilicate. Growth of epitaxial layers was conducted on setting of vertical type with a quartz reactor. Epitaxial layers were settled from gas composition of oxygen with trichlorosilane or dichlorosilane. For the alloying of a settled layer in the steam-gas composition, phosphine was imposed. For the trichlorosilane, the temperature of linings was 1490 K and the growth rate was 0.03 μm·s^{-1}, and for the dichlorosilane – 1390 K and 0.025 μm·s^{-1}.

The structural defects in the plates and ready compositions are found with the help of chrome etcher and were explored by the metallographic methods including biradial micro interferometry.

The use of interferometry method allowed to update and clarify the information about the morphology of increasing layers and the characteristic structural defects that are found with the help of selective etching, the major part of it was found with the help of metallographic microscope. Microinterferometer "МИИ-4", used while analyzing, allows making a visual value of the sample micro relief, to distinguish accurately hollows from projections and to measure their depth and height.

The analysis showed that mechanical treatment method provided the achievement of quite high quality surface. Except for periphery of the plate with the 0.5 mm width, which do, is not included in the plate area, on its other area there are not any micro roughness within the borders of separate capacity of micro interferometry method (0.03 μm). There are no spaces with residual deformation of crystal lattice within the borders of chrome etcher sensitivity. However, the edges of plates have macro and micro cracks, micro scratches up to 100 μm depth and areas with residual deformations of the lattice.

The comparing analysis of the deficiencies, which measures the plate edges after each period of treatment, allowed the authors to establish the concrete types of defects formed under operations of technological process. It is proved that chips are formed during the monocrystalline cutting for plates; while removing the broken layer on further stages of mechanical treatment, the quantity of chips, their area and depth decrease. Micro cracks appear on the stage of mechanical polishing. Chemo-mechanical polishing does not prove make any new mechanical defects on the plate edges and area. The influence of thickness and diameter of the plate and the presence of alloying impurity in initial monocrystal in the period of analyzed indexes of corresponding parameters on the deficiency character and measure in the plates is not found.

Then, the behavior of found defects of mechanical treatment under plate's effect of high temperatures was analyzed. The plates of dislocation high-resistivity silicon with 60 mm diameter and 300, 500 and 1000 μm think were given into fallout of oxygen in the atmosphere under 1450 K temperature during 10 min.

Thanks to the selective etching, the dislocations in the offshore area of plates were burnt. Authors determined that the active sources of dislocations generation were microchips on the edges of plates but micro scratches and areas with residual deformations of the lattice were extra sources of their generation on the edges of plates. The combination or generation process of dislocation by macro and microchips, micro scratches and areas with deformation bars is responsible for the appearance of the offshore circle of silicon plates 1-3 mm thick with high dislocation, density under (~ 10^3 cm^{-2}) different high temperature technological operations.

Micro cracks on the edge of plates caused the formation of gliding lines spread along the crystallographic directions at the distance up to 1 mm.

In epitaxy, the length of gliding lines that have appeared from micro cracks reaches 5, 15 mm; in some cases micro cracks initiate stage shift formation, that penetrates the whole thickness of the plate and epitaxial layer and have 0.7 diameter thick. The authors made many experimental investigations for the value of the impact of modes and improved technology on dislocation structure of semiconductor structures. These investigations were hold with the help of a microscope "МИК 4У" in reflected light increasing in the range from 600 to 1200 times (Fig. 1).

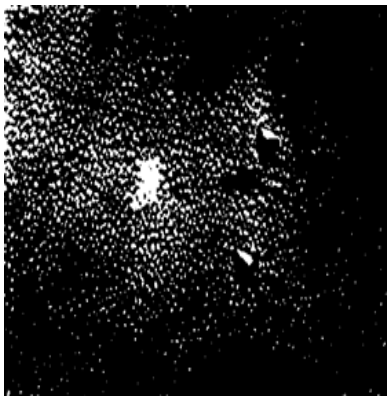
During experimental investigations, it was defined that only micro cracks influenced on the structural perfection of the working area of ready silicon compositions, and to remove such defects it was necessary to correct this operation.

For this purpose, the authors analyzed the quality of polishing on CDP-100 machines, using a separator, and on M-201 machines.

In another case, the plates were glued on the faceplate and in comparison with the first one, there was no tension on the edges while polishing.

It is determined that polishing with a free workspace on M-201 machines does not lead to the formation of micro cracks and areas with residual deformations of crystal lattice.

a



b

c

Fig. 1 – Dislocation structure of the sample on the working area of the plate (a), where defects of mechanical treatment were absent; the dislocation formation during burning was shown only in the plates that had microdefects of A-type (b); having micro defects of another types, the working area of the plates was free from dislocations (c)

Use of the linings treated according to the above-mentioned technology doing the operations of mechanical polishing on M-201 machines, allowed removing gliding lines and stage shift under epitaxial increasing not only of one layer silicon structures (time of deposition is about 15 min), but also of wrapped silicon structures (2, 3 hours). The efficiency of M-201 machine is much lower than CDP-100; that is why they can recommend the first one only in the cases, when demands to structural perfection of epitaxial compositions are present. The raising of temperature causes a great impact of defect formation in epitaxial structures on electrical characteristics and parameters of photoelectrical converters and on the quality of their contact systems that must have high electro safety in exploitation. The authors have proposed the optimal mode of contact systems production, of contact resistance and stability of Al, Al-Cu and Al-Cu-Si contacts.

The investigations were done on special test structures of 3.8×6.35 μm² size. The plates were 76 mm diameter and 500 μm thick; Al, Al-Cu (2 %) and AL-Cu (2%)-Si (1 %) metallization, 0.8 μm thick with applied on the relevant sets of plates.

Directly before deposition, the plates were polished in HF solution (concentrate) for 30 s, after etching they were washed in hot, then in cold distilled water, washed in alcohol and dried in thermostat.

After that, plates were placed in the working chamber of magnetron sputtering device. The interval between treatment operations of the linings and their downloading into the working chamber was 30 min.

After formation of given metallization topology, the plates were burnt in nitrogen under 450 °C temperature during 15 min, and a protective SiO_2 layer of 0.9 μm thick was applied. Then oxide was removed and divided into separate crystals. The test crystals installation into the body was made using Au-Ge alloy [3].

At the finish stage, diversion was welded to diversion areas with ultrasonic method and resealed a test module with the glass under 450°C-500 °C. The average index of contact resistance obtained from 20 measurements for every metallization type is given in Table 1.

Table 1 – The average index of contact resistance for different metallization types

Metallization type	Contact resistance, Ohm
Al	2.80 ± 0.1
Al-Cu	6.45 ± 2.08
Al-Cu-Si	4.82 ± 1.60

The further development of PC on the basic epitaxial composition is connected with improvement of production technology and stabilization of their parameters. The main task of producers nowadays is to increase the PC efficiency, to improve the production technology and to reduce the price of materials.

4. CONCLUSIONS

The optimal mode of contact systems production for PC on silicon epitaxial structures was proposed, and the analysis of contact resistance and stability of Al, Al-Cu and AL-Cu-Si contacts that had higher persistence to electro migration and at the same time removed silicon erosion in the contact windows was hold. It is proven, that temperature significantly affects the defect formation in epitaxial structures on electrical characteristics and parameters of PC, as well as on the quality of contact systems, which should have a high thermal conductivity, mechanical strength and reliability in operation. Defined voltage mismatch occurs directly in the process of building epitaxial layer at a temperature of crystallization, i.e. at maximum temperature in the

system, so there is a large probability of their relaxation in the process deposition with formation of dislocations not matching and other defects. Found that the thermal stress in epitaxial structures is able to cause the difference between the coefficients of thermal expansion of materials, which are combined, and uneven distribution of temperatures within the extended layer.

Thus, the voltage mismatch can depend on their size, as well as the mechanical properties of the material, and the growing conditions lead to an elastic or plastic deformation or mechanical destruction. We should also note that the main reason for the occurrence of dislocations is the difference in lattice periods.

The behavior of found defects on the plate under high temperatures and the ways of their removing was analyzed. It would lead to the improvement of PC quality, using their efficiency, lowering the energy cost and increasing the strength to special conditions.

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Вплив дефектів на якість контактних систем для фотоелектричних перетворювачів

О.Ю. Небеснюк, З.А. Ніконова, А.О. Ніконова, С.Л. Хрипко

Інженерний інститут Запорізького національного університету, пр. Соборний., 226, 69006 Запоріжжя, Україна

Енергія є ключовим фактором, а також знаходиться у центрі економічних, соціальних та екологічних завдань сучасного розвитку. У статті запропоновано напрями поліпшення якості традиційних, а також освоєння нових напівпровідникових матеріалів і різних типів металізації. Особливо великі перспективи обіцяє застосування епітаксійних композицій для виготовлення фотоелектричних перетворювачів. Чітко проявляються тенденції створення найскладніших електронних пристроїв на основі багатошарових епітаксійних структур. При цьому формуються дуже високі вимоги до електрофізичних властивостей і досконалості структури кожного шару, ставляться завдання створення якісних та різких p-n переходів і гетеромеж на великих площах епітаксійних композицій.

Ключові слова: Пластина, Дефекти, Епітаксійні композиції, Контактні системи, Фотоелектричні перетворювачі.