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Influence of Tunable Work Function on SOI-based DMG Multi-channel Junctionless Thin Film Transistor

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This paper focuses on the effects occurring due to the inclusion of multi-channel titanium nitride (TiN) material in a dual metal gate (DMG) junctionless (JL) thin film transistor. Two nanosheets have been implemented in a JL tri-gate transistor, which is separated by the gate oxide layer and surrounded by the gate layer. The thickness of TiN material placed in between the gate oxide and gate layer helps in tuning the work function of the gate. The comparison has been done between single channel with single metal gate, double channel with single metal gate, double channel with DMG and double channel with DMG and TiN. Strains have been created in the devices by implementing TiN and DMG. An improvement of 31 % in the output current has been obtained using DMG double channel device when compared with single gate single channel device. The comparison has been carried out in Sentaurus technology computer aided design (TCAD). The drift diffusion model, the mobility model, which includes the effects of doping concentration and electric field, the bandgap narrowing model and the Shockley-Read-Hall recombination model have been used to calculate outputs. The proposed structure acquires higher transconductance values than normal tri-gate devices. It has been verified that when varying the TiN thickness, the potential has been tuned. Due to the tuning of the work function, the performance of the device has been improved.

Keywords: Junctionless tri-gate transistor, Multi-channel, TiN, Dual metal gate (DMG), Thin-film transistor, SOI.

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1. INTRODUCTION

In recent years, researchers have focused on utilizing the benefits of a junctionless (JL) thin film transistor device due to its ease in fabrication and lower thermal budget issues than regular devices. The first JL nanowire transistor was made in 2010 [1]. The JL concept was later implemented in several devices, such as gate-all-around, FinFET, tunnel FET, thin film transistor, double gate and tri-gate devices. These devices have strong immunity against subthreshold operations like subthreshold slope (SS) and leakage current when scaled down to nanolevels [2, 3]. High-performance thin film transistor devices are favorable for Active-Matrix Organic Light-Emitting Diode (AMOLED) and Active-Matrix Liquid-Crystal Display (AMLCD).

There is an increase in the drain current and transconductance of a JL transistor due to its dual metal gate (DMG) formation [4, 5]. The gate region is formed with two metals having different work functions. The difference in work functions of metals causes the potential step to change near the junction, as a result of which the carrier velocity, carrier transport efficiency and drain current are increased [6]. In the DMG structure, the peak electric field at the drain end is reduced. This causes a reduction in hot carrier effect at the drain side, which creates a rise in the average electric field under the gate. There is a reduction in the ability of localized charges to increase drain resistance, due to which their lifetime is increased [7, 8]. In [9], by building DMGs in cylindrical nanowires and analyzing with various gate oxides, the superiority of HfO_2 dielectric over other oxide layers has been established. The efficiency of DMG relies on its work function. And hence instead of replacing alternative metals with increased work functions, titanium nitride (TiN) material is incorporated in between the gate and dielectric to tune the work function. The work function of TiN metal gate can be tuned by varying the thickness of the TiN layer. The cost of fabrication for each metal gate can be reduced. [10, 11] discuss the tuning of the work function using TiN and titanium silicon nitride (TiSiN) for FinFET and FDSOI transistors. The work function increases with increasing nitrogen content.

Other than the DMG and TiN functionality, one of the best options to increase the current flow is through vertical stacking of channels. The vertical stacking could be attained without having to increase the area in the lateral direction or degrading the performance of the already existing device [12]. Multi-channel MOSFET is a strong contender for devices having vertically stacked channels. The concept of stacking of multiple channels in a planar MOSFET has been conveyed in [13, 14], and in [15] for thin film transistors and JL thin film transistors. The number of channels being split from a single channel could determine the high current drivability of the device. In this work, a silicon on insulator (SOI) based nanosheet has been formed, where a multi-channel is replaced for a single channel. HfO_2/TiN/dual metal tri-gate structure is formed around the channels, instead of using a single metal tri-gate. This work could mainly be explained in terms of its gate engineering technique, i.e. TiN layer placed in between the gate and dielectric layers. The device parameters and tuned potential are evaluated by varying the thickness of TiN.

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2. DEVICE STRUCTURE

A JL thin film transistor has been formed and simulated in the TCAD simulation tool, as shown in Fig. 1, by using the parameters that have been taken from [1].

Since the device was formed on SOI, the channel was surrounded by tri-gate. The channel thickness and width are respectively 10 nm and 20 nm, and the gate length is 1 μm. A doping concentration of $2 \cdot 10^{17}$ is applied uniformly throughout the source, drain, and channel. SiO_2 was chosen as a material for both gate oxide and buried oxide layers. The device was simulated by keeping V_{GS} at 1.3 V and V_{DS} at 1.5 V. Fig. 2 shows that simulated results match with the experimental ones [1]. Fig. 3 shows the structure of the vertically stacked double channel and DMG in a JL thin film transistor, which are separated and surrounded by HfO_2. Similar dimensions and doping concentrations utilized for a single-channel were used here, other than inter-oxide layer thickness. Single metal gate was replaced by DMG, and the work functions for metal 1 and metal 2 were 4.8 eV (gold) and 4.33 eV (titanium), respectively, considering the values from [16]. The length for both metals was 500 nm [17]. The incorporation of TiN material in between the gate and HfO_2 layer [11] is also represented in Fig. 3. The addition of TiN material, MBC structure, and DMG to a thin film transistor was explained through its fabrication steps in [1, 5-7, 11, 13-15].

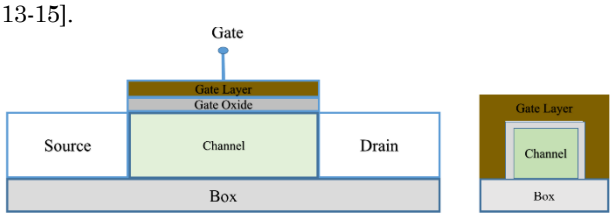

Fig. 1 – Tri-gate nanosheet on SOI

The physical models used for simulation of the structure in Fig. 1 for calibration purposes are the drift diffusion model, mobility model which includes the effects of doping concentration and electric field, bandgap narrowing model and Shockley-Read-Hall recombination model. Additionally, the following model was used for other structures: the high field saturation model for calculating velocity saturation. The carrier-carrier scattering model was also applied in the simulation. The CVT mobility model was used because it considers parallel and perpendicular field dependent mobility. The hot carrier injection model was involved to calculate hot carrier injection [18, 19].

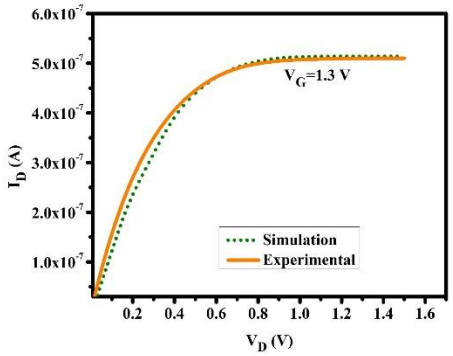

Fig. 2 – Simulation result matches the experimental data [1]

3. RESULTS AND DISCUSSION

3.1 Electric Potential

Fig. 4 shows the variation of the electric potential between single channel with single metal gate, double channel with single metal gate, and double channel with DMG. The potential under metal 1 will be lower compared to 2, since metal 1 has a higher work function than metal 2.

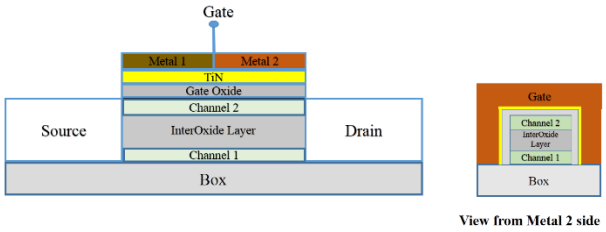

Fig. 3 – DMG, multi-channel and TiN implementation in dual metal tri-gate thin film transistor

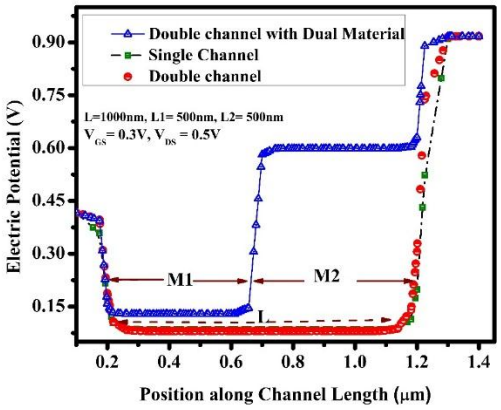

Fig. 4 – Electric potential variation in single metal gate and DMG

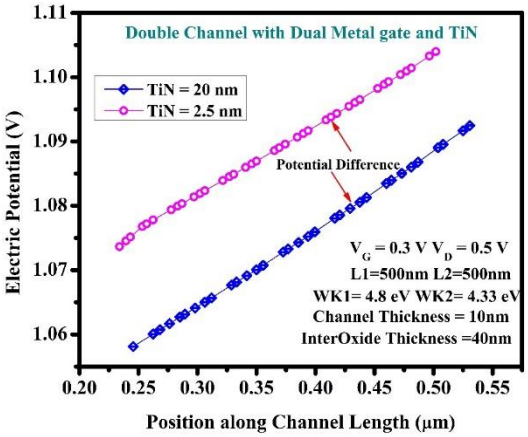

Fig. 5 – Electric potential variation in double channel with DMG with TiN

Both are connected laterally, so electrons can easily pass from the source to the channel side. The sudden difference in work functions near the junction of two metals creates a step potential in that region, and the average carrier velocity increases due to that functionality. This explains the continuity of potential at the interface region. In [11], a study was performed on TiN

with a mid-gap work function that can be tuned by the varying thickness of TiN metal in the device. [11] experimentally proved a work function modulation of 100 meV, which could further achieve about 250 meV by varying the thickness from 2.5 nm to 20 nm, after which it will be saturated. After incorporating TiN in the double channel with DMG device, as structured in Fig. 3, the electric potential has been analyzed by varying the thickness of TiN from 2.5 nm to 20 nm, whose results have been plotted in Fig. 5. The relationship between the work function and potential is $WF = -q\Phi - EF$. So, with increasing TiN thickness, the work function increases, and the potential decreases. The thickness of TiN increases from 2.5 nm to 20 nm. The potential also decreases, which proves the tuning of the work function in meV. The potential has been tuned around 12 mV, when the TiN thickness varied from 2.5 nm to 20 nm. The work function engineering has been explained well in [9].

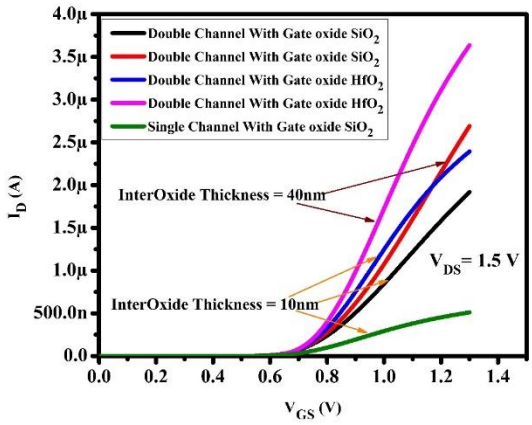

Fig. 6 – Transfer characteristics of double channel single metal gate and single channel single metal gate with different inter-oxide thickness

3.2 Drain Current

As given in Fig. 3, a double channel structure is formed with the inter-oxide layer and analyzed with a single channel structure. The transfer characteristics are plotted in Fig. 6 based on the thickness of the inter-oxide layer.

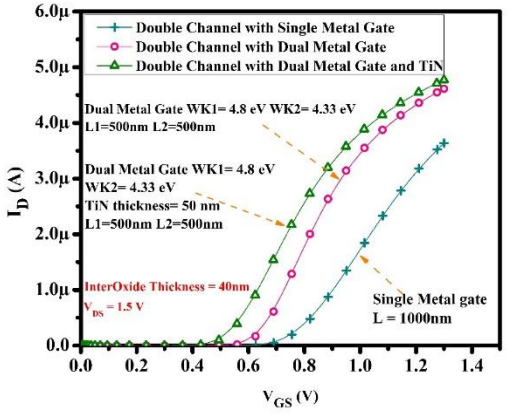

Fig. 7 – Comparison of the transfer characteristics of double channel with single metal gate, double channel with DMG and double channel with DMG and TiN

V_{DS} is kept as a constant voltage of 1.5, and V_{GS} is varied from 0 to 1.3 V. The graph is plotted for inter-oxide values of 10 nm and 40 nm with gate oxide layers of both SiO_2 and HfO_2. A maximum inter-oxide thickness of 40 nm was considered for evaluation since the drain current reduces beyond that scale. As suggested in [9], HfO_2 has a better performance than SiO_2. With an increase in the thickness of the inter-oxide layer, the drain current enhanced oxide capacitance.

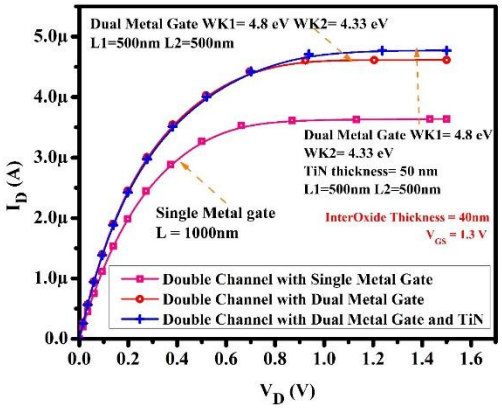

Fig. 8 – Comparison of the output characteristics of double channel with single metal gate, double channel with DMG and double channel with DMG and TiN

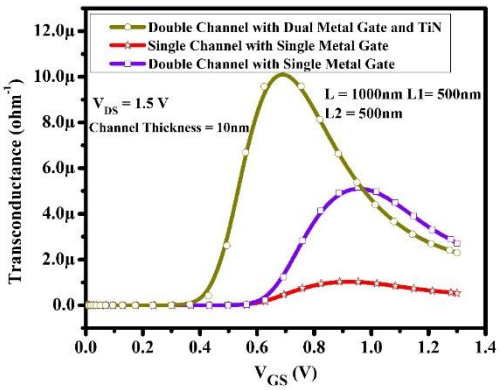

Fig. 9 – Variation of transconductance with different devices

Fig. 6 deals with the single metal gate with double channel, whereas Fig. 7 and Fig. 8 explain the double channel with single metal gate, double channel with DMG, and double channel with DMG and TiN. Transfer characteristics are plotted by taking V_{DS} at 1.5 V and varying V_{GS} from 0 to 1.3 V. The output characteristics are drawn by keeping V_{GS} at 1.3 V and varying V_{DS} from 0 to 1.5 V. Here the inter-oxide thickness is taken as 40 nm for all the devices, and TiN thickness is taken as 2 nm in the double channel with DMG and TiN. Both graphs show that DMG increases the velocity of carriers and eventually increases the drain current. When TiN is included in the device, the current furthermore increases because of tunable work function. Fig. 9 shows the comparison of transconductance for various devices. Even though the MBC structure increases the current compared to single channel, inclusion of DMG and TiN increases the transconductance than double channel single metal gate JL thin film transistor. I_{on}/I_{off} was calculated for all the devices.

The single channel device given in [1] has an I_{on}/I_{off} ratio of larger than 10^6, whereas the double channel with DMG has an I_{on}/I_{off} ratio of around ~ 10^8. The double channel with DMG and TiN achieves an I_{on}/I_{off} ratio of ~ 10^6. Fig. 10 shows the comparative analysis of different structures used in this work. Fig. 10 also shows the proposed structure having about 9.4 times better drain current than the single channel device [1].

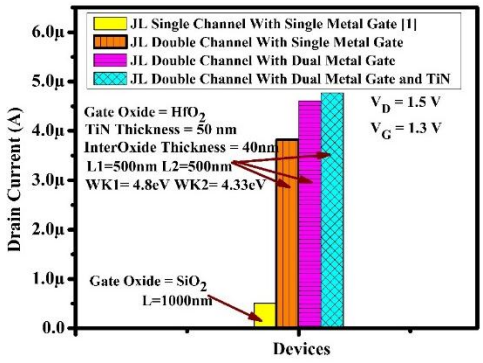

Fig. 10 – Drain current comparison of single metal gate with single channel, double channel with single metal gate, double channel with DMG and double channel with DMG and TiN

4. CONCLUSIONS

A JL thin film transistor device was formed by integrating TiN over the DMG, MBC structure with double channels. The device performance was later compared with single metal gate and DMG structures with JL double channel. Based on the MBC structure, DMG phenomena and tunable TiN work function, the performance increased in the device. The effects of interoxide thickness and electric potential were analyzed. Around 12 mV potential modulation was achieved by varying TiN thickness. The accurate nature of the outcomes proves the device potential to build AMOLED based devices in the future.

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