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Influence of Triple Material on Performance Study of Double Gate PiN Tunneling Graphene Nanoribbon FET for Low Power Logic Applications

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Influence of triple material having different work functions have been designed and investigated on a double gated P-i-N tunneling graphene nanoribbon field effect transistor (DG-TM-PiN-TGNFET) for improved device performance. A III/V compound material (InAs) has been used in the source region for this *n*-channel heterojunction tunnel FET, because of which stress – strain effect results better tunneling. Graphene, being a low band gap material, has been used as nano ribbon to tune suitably the energy bandgap as less as possible. In this paper, the three different materials are introduced to restrict the drain – source reverse tunneling and also improve the TFET device performance in terms of surface potential distribution, lateral – vertical electric field variation and transfer characteristics. This triple material-based DG-PiN-TGNFET structure provides better subthreshold swing of 18.56 mV/decade at 0.5 V supply voltage compared to single and double material based double gated TGN-FET structures. The entire simulation has been performed using two-dimensional mathematical TCAD device software. Moreover, the low threshold voltage encourages the proposed device best suitable for low power logic applications.

Keywords: Work function, DG-TM-PiN-TGNFET, III/V Compound material, Surface potential, Reverse tunneling, TCAD.

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1. INTRODUCTION

The conventional complementary metal oxide semiconductor (CMOS) technology for integrated circuit (IC) fabrication, has been outplayed due to device dimension scaling issues [1]. Since in todays' era, the device scaling has been travelled from millimeter range to nanometer range, therefore short channel effects (SCE) restrict further downscaling of CMOS transistors [2, 3]. Due to the fundamental limitation of subthreshold swing (SS), the CMOS devices cannot produce high drive current at low threshold voltage (V_{th}). In addition, the rising OFF-state leakage current with respect to device node technology limits its further usage. Therefore, a new device physics has been introduced in nano-device modelling called tunnel field effect transistors (TFET). This device having typical gated P-i-N (*p* type – Intrinsic – *n* type) junction diode structure incorporates band-to-band (BTBT) quantum tunneling, unlike MOS transistors. This results low subthreshold swing (less than 60 mV/decade in room temperature for MOSFETs) and better control in SCE and further drain induced barrier lowering (DIBL) issues [4-6]. In spite of these advantages, TFET devices meet considerable challenges in producing better ON-state current (I_{ON}). To overcome this problem, several typical device structures with gate and material engineering have been studied [7-14]. Moreover, the supply voltage (V_{DD}) needs to be lowered with device downsizing for low power applications. After undergoing a thorough literature surveys of recent times [15-20], graphene nanoribbon has been introduced over Si channel. Graphene, being an excellent mechanical and electronic property holder; has been used as nanoribbon to tune the energy band gap and thereby enhancing the switching ratio (I_{ON}/I_{OFF}).

2. DEVICE STRUCTURE

In this section, the established device structure of an *n*-type double gate dual material P-i-N tunneling graphene nanoribbon field effect transistor (DG-DM-PiN-TGNFET) [21] is shown in Fig. 1.

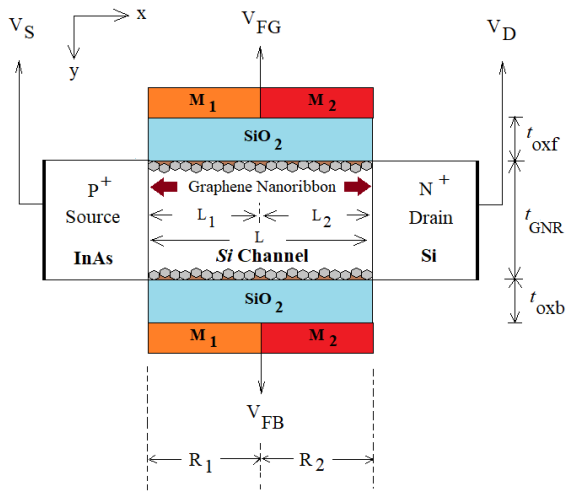

Fig. 1 – Two-dimensional lateral structure of InAs/Si heterojunction DG-DM-PiN-TGNFET

In the presence of ultra-thin graphene layer over *Si* channel of proposed heterostructure (InAs/Si), the carrier transport results better I_{ON}, I_{ON}/I_{OFF} ratio and subthreshold swing (SS) compared to other advanced double gated TFET. Here front and back gate are connected to two metals (M_1 and M_2) of different work-function ($\phi_{M1} = 4.5$ eV, $\phi_{M2} = 4$ eV). The lengths of M_1 and M_2 are $L_1 = 10$ nm and $L_2 = 10$ nm, respectively,

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hence L is the total effective channel length of 20 nm. The gate oxide thickness both at front and back gate (t_{oxf} and t_{oxb}) are of 2 nm each, whereas the body thickness (t_{GNR}) is considered as 10 nm. The doping at source, drain and channel regions are considered as $N_S = 10^{20}$ cm^{-3}, $N_D = 5 \times 10^{18}$ cm^{-3} and $N_{ch} = 10^{16}$ cm^{-3}. Now the similar structure has been modified with an additional material (M_3) having work function ($\phi_{M3} = 4.8$ eV) in order to achieve better drain current (I_{ON}) and steep subthreshold slope compared to the earlier. The modified n-type double gate triple material P-i-N tunneling graphene nanoribbon FET (DG-TM-PiN-TGNFET) is shown in Fig. 2. To make equal comparison between these two device structure dimensions, the channel length (L) has been considered same as 20 nm, where the individual lengths of three materials (M_1, M_2, M_3) are $L_1 = 5$ nm, $L_2 = 10$ nm and $L_3 = 5$ nm. Though, the width of dielectric and body remain unaltered and so as the doping concentrations at source, drain and intrinsic channel regions [22].

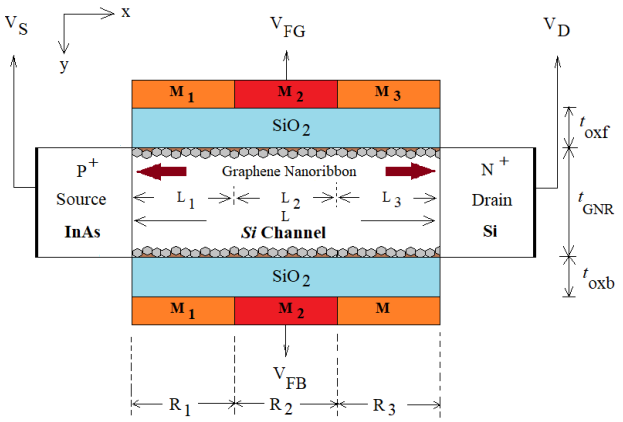

Fig. 2 – Two-dimensional lateral structure of InAs/Si heterojunction DG-TM-PiN-TGNFET

3. SIMULATION METHODOLOGY

The double gated P-i-N tunneling TGNFET with double and triple material have been simulated and designed using non-linear numerical device simulator - SILVACO TCAD software [23]. The simulated results are graphically plotted and thoroughly compared for better device performance with low power consumption. Shockley Read and Hall (SRH) model is used for recombination effects, Band gap narrowing (BGN) model is used for high doping and BTBT model is used for band-to-band tunneling. Non-local BTBT model is used here in our work.

4. RESULTS AND DISCUSSION

In this section, all TCAD simulated results have been analyzed and discussed.

4.1 Energy Band Diagram

Due to the incorporation of compound (III/V) material like, Indium Arsenide (InAs) at source region of n-type TFET; the BTBT tunneling rate is increased much higher in this hetero-structure compared to all Silicon material (Si) homostructure. The ultrathin barrier can be easily tunneled through for InAs/Si heterojunction. The related energy band diagram is shown in Fig. 3.

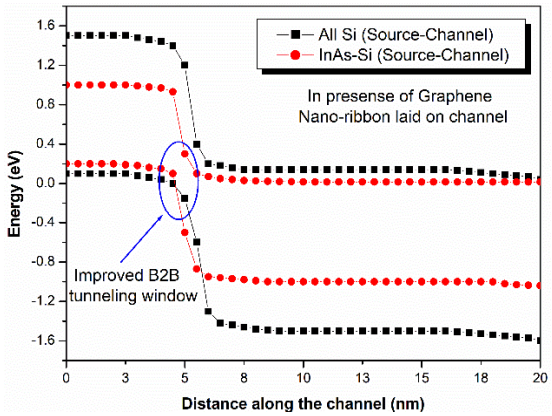

Fig. 3 – Energy band diagram comparison between InAs/Si and Si/Si based DG-TM-PiN-TGNFET

4.2 Surface Potential Distribution

The surface potential distribution laterally along the channel region can be analyzed graphically, as shown in Fig. 4. Here, the proposed TGNFET structure produces better peak at source – channel interface for DG-TM-PiN-TGNFET. Moreover, the potential distribution of both device models has been designed at 0.5 V supply voltage.

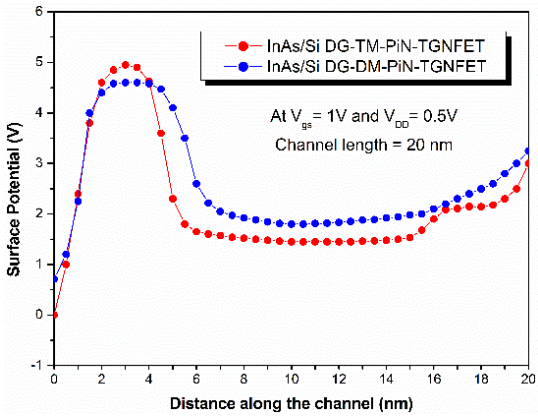

Fig. 4 – Surface potential distribution comparison between DG-DM-PiN-TGNFET and DG-TM-PiN-TGNFET

4.3 Electric Field Variation

Since there are two electric fields generated after biasing, therefore both the electric fields i.e., lateral electric field (E_x) distribution and vertical electric field (E_y) distribution have been plotted in Fig. 5 and Fig. 6, respectively.

The incorporation of third material (M_3) ensures the better spike in lateral electric field variation along channel length. However, since the width of all layers have been considered same for both the device structures; therefore, the vertical electric field variation remains almost equivalent to each other.

4.4 Transfer Characteristics

The ON-state and OFF-state current variation is

plotted against gate-source voltage (V_{gs}). As the threshold voltage (V_t) reduction is the main challenge for low power consumption, therefore the double gated P-i-N TGNFET plays vital role to achieve it. From Fig. 7 it can be clearly determined that the influence of third material (M_3) significantly reduces the subthreshold swing (SS) recorded at 18.56 mV/decade. Whereas, using dual material used in DG-DM-PiN-TGNFET, the swing achieved as 21.94 mV/decade and in DG-SM-PiN-TGNFET, it provides 30.81 mV/decade at supply voltage of 0.5 V.

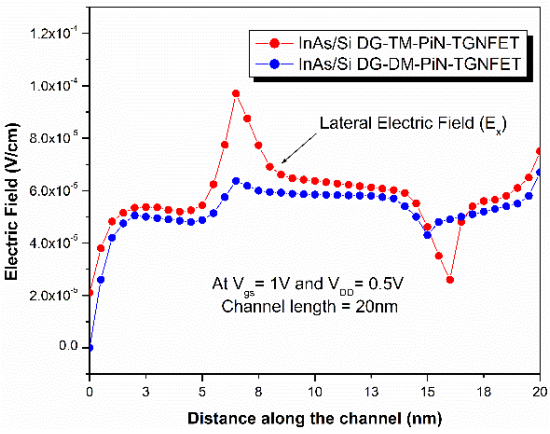

Fig. 5 – Lateral electric field variation of DG-DM-PiN-TGNFET and DG-TM-PiN-TGNFET at V_{DD} = 0.5 V

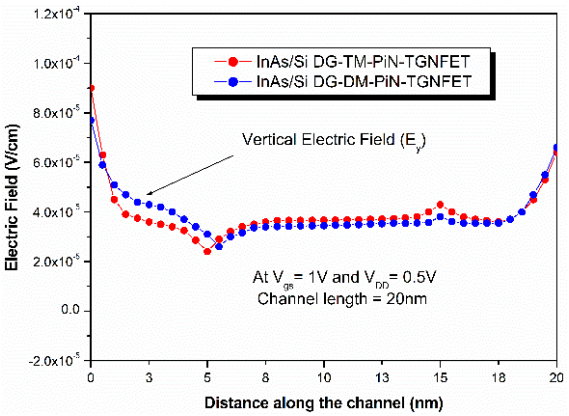

Fig. 6 – Vertical electric field variation of DG-DM-PiN-TGNFET and DG-TM-PiN-TGNFET at V_{DD} = 0.5 V

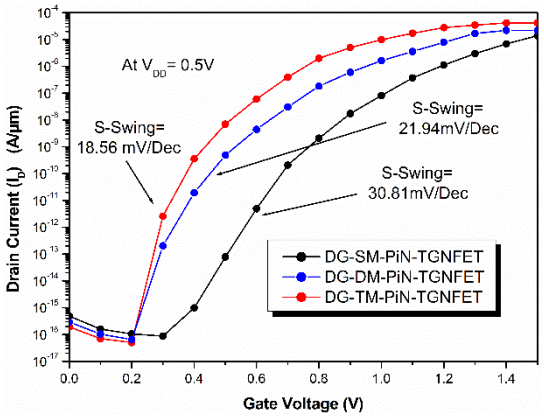

Fig. 7 – Transfer characteristics of various device structures of DG-SM-PiN-TGNFET, DG-DM-PiN-TGNFET and DG-TM-PiN-TGNFET at V_{DD} = 0.5 V

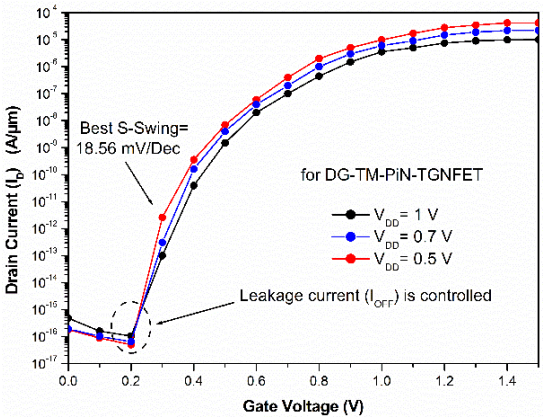

Fig. 8 – Drain current variation of DG-TM-PiN-TGNFET at different supply voltages (V_{DD} at 0.5 V, 0.7 V and 1 V)

Moreover, the leakage current (I_{OFF}) has also been controlled considerably for proposed DG-TM-PiN-TGNFET structure.

In this paper, the main contribution to this established novel device structure is the triple material implementation. For low power logic application, the triple material-based DG-PiN-TGNFET provides best I_{ON}, I_{ON}/I_{OFF} ratio and subthreshold swing. In Fig. 8, it can be analyzed that DG-TM-PiN-TGNFET provides best subthreshold swing at V_{DD} = 0.5 V. Moreover, better turn-on voltage (V_{ON}) has been achieved. The leakage current (I_{OFF}) is also get controlled at V_{DD} = 0.5 V.

5. CONCLUSIONS

This work is prepared mainly for low power logic applications. The static power dissipation becomes almost zero when the transistor is switched OFF. But while switching ON, the dynamic power dissipation becomes directly proportional to V_{DD}. So, the V_{DD} need to be minimized w.r.t. device downscaling. If V_{DD} does not decrease yet device dimensions were decreased, then these leads rise in leakage current (I_{OFF}).

To overcome this issue, the novel lateral structure of DG-TM-PiN-TGNFET has been proposed and the influence of triple material (M_3) has been categorically showcased in results and discussion section. The energy band diagram, surface potential distribution, electric field variation (lateral and vertical) and transfer characteristics of proposed DG-TM-PiN-TGNFET has been obtained and compared with DG-DM-PiN-TGNFET and DG-SM-PiN-TGNFET. Low subthreshold swing and better I_{ON} at low V_{th} has inspired the triple material-based DG-PiN-TGNFET to operate in low power logic applications.

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Вплив потрійного матеріалу на дослідження продуктивності тунельного польового транзистора з графенових нанострічок PiN FET з подвійним затвором для додатків низькопотужної логіки

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Було розроблено потрійні матеріали з різними роботами виходу та досліджено їх вплив на роботу тунельного польового транзистора з графенових нанострічок PiN FET з подвійним затвором (DG-TM-PiN-TGNFET) для підвищення продуктивності пристрою. Складений матеріал III/V (InAs) був використаний в області витоку цього тунельного польового транзистора з n-канальним гетеропереходом, завдяки чому напружено-деформований стан покращував тунелювання. Графен, який є матеріалом із невеликою шириною забороненої зони, був використаний у формі нанострічки, щоб максимально зменшити ширину забороненої зони. У роботі представлено три різні матеріали для обмеження зворотного тунелювання між стоком та витоком, а також для покращення продуктивності тунельного транзистора з точки зору розподілу поверхневого потенціалу, поперечно-вертикальних змін електричного поля і передавальних характеристик. Ця DG-PiN-TGNFET структура на основі потрійних матеріалів забезпечує кращі підпорогові коливання амплітудою 18,56 мВ/декада при напрузі живлення 0,5 В у порівнянні з TGN-FET структурами з подвійним затвором на основі одинарних та подвійних матеріалів. Повне моделювання було виконано за допомогою програмного забезпечення для розв'язування двовимірних математичних задач TCAD. Більше того, низька порогова напруга сприяє тому, що пропонований пристрій найкраще підходить для додатків низькопотужної логіки.

Ключові слова: Робота виходу, DG-TM-PiN-TGNFET, Складений матеріал III/V, Поверхневий потенціал, Зворотне тунелювання, TCAD.