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# Impact of Device Sizing on Electrical Properties of DG-SOI-MOSFET Using Octave Software

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Double-gate (DG) SOI-MOSFET device is regarded as the next generation of VLSI circuits. In this paper, we show the impact of miniaturization on the demand and challenges of the undoped-body symmetric DG-SOI-MOSFET planar design for low power and high performance. By exploiting the graphical approach used previously, which consists of numerical simulations valid for all bias conditions, from subthreshold to strong inversion and from linear to saturation operation, we visualized the evolution of the transfer, output and electrical characteristics and output conductance by varying each of the parameters independently: oxide thickness ($t_{ox}$), channel length ($L$) and channel width ($W$). The results obtained allowed to verify how each dimension affects different electrical properties of the DG-SOI-MOSFET. It was found that $L$, $W$ and $t_{ox}$ significantly influence these properties, as well as this transistor includes the channel length-modulation (CLM) and drain induced barrier lowering (DIBL) effects. This study showed the ability to predict the electrical behavior of the DG-SOI-MOSFET by its geometrical dimensions, and the possibility of choosing the optimal dimensions to ensure high performance of this transistor in both analog and digital circuits.

**Keywords:** Symmetrical DG-SOI-MOSFET, Electrical characteristic, Conductance, Miniaturization, Numerical method.

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## 1. INTRODUCTION

The double-gate (DG) MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology [1, 2]. However, conventional device structures, such as bulk MOS transistors, are approaching fundamental physical limits [3]. In this regard, SOI technology has demonstrated many advantages over bulk silicon technology, such as low parasitic junction capacitance, high soft error immunity, elimination of CMOS latch-up, no threshold voltage degradation due to body effect and simple device isolation process [4]. The advantages of DG-SOI-MOSFETs come at the expense of an additional gate (back gate), leading to high gate capacitance, dual leakage channels, and tricky front- and back- gate coupling, which complicates circuit design [5]. The absence of dopant atoms in the channel eliminates impurity scattering mobility degradation and completely does away with unwanted dispersion in the characteristics, otherwise resulting from the random microscopic dopant fluctuations inherent to ultra-small dimensions devices. In fact, the threshold voltage is determined by the work function difference between the gate material and the intrinsic silicon body [6]. On the other hand, symmetrical DG-SOI-MOSFETs appear to be attractive alternatives as they can effectively reduce short channels effects and work under higher currents [7].

In this article, we want to continue to validate the model developed previously [8], which will be applied to nanoscale symmetric DG-SOI-MOSFETs. The output and transfer characteristics and output conductance will be determined for various gate polarizations, channel lengths, oxide thicknesses and silicon film thicknesses.

## 2. OUTPUT AND TRANSFER CHARACTERISTICS

As a first step, the Poisson equation and associated boundary conditions lead to a transcendental equation that will allow to find the electrostatic potential at the center of the silicon film. Knowing this electrostatic potential, it is easy to calculate the potentials on the surface and in the volume and obtain the electrical charge carrier density in the channel [8]. Our model uses only the drift current component, which is broadly acceptable as the diffusion component, first proposed by Pao and Sah, is only a few percent of the total drain current [9].

For the analytical calculation of electric current, we have followed the steps below. Neglecting the scattering component and considering a constant electron mobility of about 0.03 m²/Vs throughout the silicon film, the drain current is calculated using expression (1):

$$I_D = \mu \cdot \frac{W}{L} \cdot \int_0^{V_{DS}} Q_{inv}(V)\,dV\,. \tag{1}$$

The DG-SOI-MOSFET device is symmetrical. It is not doped. The charge induced in the channel is practically equal to the total charge in the semiconductor. Therefore, by applying Gauss's law to the interfaces and replacing the inversion charge $Q_{inv}$ by its expression (2), the drain current $I_D$ is written as:

$$I_D = \mu \cdot \frac{W}{L} \cdot \sqrt{8\varepsilon_{Si} n_i KT} \times \\ \times \int_0^{V_{DS}} e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot \left| \tan\left(be^{\frac{q(\varphi_0 - V)}{2KT}} \cdot \frac{t_{Si}}{2}\right) \right| dV. \tag{2}$$

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After the calculation and taking into account the assumptions we have imposed, we get:

$$I_D = \mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[ V_{GS} \cdot V_{DS} - \int_0^{V_{DS}} \varphi_S(V) dV \right]. \quad (3)$$

## 3. CONDUCTANCE OF THE SYMMETRICAL DG-SOI-MOSFET

By definition, the output conductance of a MOSFET is the ratio of the change in the drain current to the change in the drain voltage, when the gate voltage is kept constant. The output conductance is written as:

$$g_{out} = \left( \frac{\partial I_D}{\partial V_{DS}} \right) V_{GS} = \text{constant} . \quad (4)$$

Substituting expression (3) into (4), after the calculation, we obtain the analytical expression for the output conductance $g_{out}$:

$$g_{out} = 2\mu \cdot \frac{W}{L} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[ V_{GS} - \frac{\partial}{\partial V_{DS}} \left( \int_0^{V_{DS}} \varphi_S(V) dV \right) \right]. \quad (5)$$

## 4. RESULTS AND DISCUSSION

In order to examine the effect of sizing on the characteristics of the components, by exploiting the graphical approach, we fixed the doping concentration of the silicon channel $N_A = 10^{15}$ cm$^{-3}$, doping concentration of source/drain contact regions $N_D = 10^{20}$ cm$^{-3}$ and mid-gap metal gate with work-function 4.74 eV. We also visualized the evolution of the transfer, output electrical characteristics and output conductance by varying each of the parameters independently: the oxide thickness ($t_{ox}$), thickness ($t_{Si}$), length ($L$) and width ($W$) of the channel. All of the device parameters are shown in Table 1.

**Table 1** – Sizing parameters

| | |
|---|---|
| Oxide thickness $t_{ox}$ | 1, 2, 3 nm |
| Channel length $L$ | 25-30-35 nm |
| Channel width $W$ | 25-50-75 nm |

The results obtained through numerical simulation using the graphical approach in Octave software are shown in the following.

### 4.1 Effects of Changing Oxide Thickness ($t_{ox}$)

By varying the oxide thickness (1, 2, 3 nm), Fig. 1 and Fig. 2 represent, respectively, the output characteristics $I_{DS} = f(V_{DS})$ and output conductance $g_{out} = f(V_{DS})$, and transfer characteristics $I_{DS} = f(V_{GS})$ of our transistor. By observing these characteristics, it is easy to notice that the current $I_{DS}$ and the output conductance $g_d$ are inversely proportional to the oxide thickness ($t_{ox}$).

On the curves of the $I_{DS}$-$V_{GS}$ characteristics, we notice that $V_{th}$ strongly depends on this thickness and increases when $t_{ox}$ increases. On the other hand, an abnormally large oxide thickness for structures with small geometries results in the isolation of the gate which no longer controls the channel.

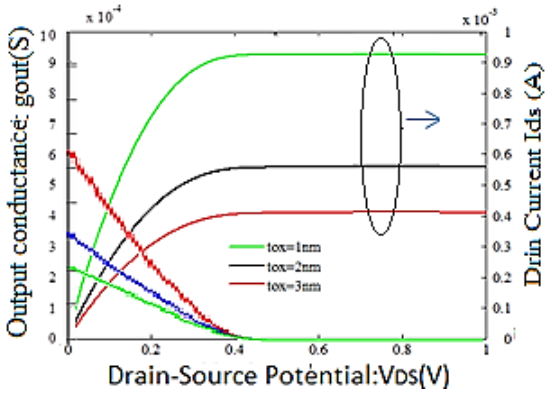


**Fig. 1** – Output characteristics and output conductance $I_{DS}$ and $g_{out}$ vs $V_{DS}$ for different oxide thickness ($t_{ox}$)

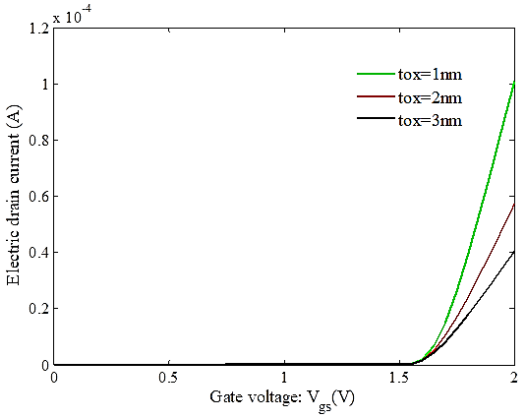


**Fig. 2** – Transfer characteristics $I_{DS} = f(V_{GS})$ for different oxide thickness ($t_{ox}$)

### 4.2 Effects of Changing Channel Length ($L$)

Fig. 3 and Fig. 4 represent, respectively, the output characteristics $I_{DS} = f(V_{DS})$ and the output conductance $g_{out} = f(V_{DS})$ and transfer characteristics $I_{DS} = f(V_{GS})$ of DG-SOI-MOSFET for different channel lengths $L$ (25, 30 and 35 nm).

Again, in these figures, it is easy to notice that the current $I_{DS}$ and the conductance $g_d$ are inversely proportional to the length of the channel $L$. The output conductance and Early voltage are severely affected by length scaling as channel length-modulation (CLM) and drain induced barrier lowering (DIBL) effects become more important, but they are acceptable for channel lengths above 15 nm [10].

### 4.3 Effects of Changing Channel Width ($W$)

By varying the channel width $W$ (25, 50 and 75 nm), we found the output characteristics $I_{DS} = f(V_{DS})$, output conductance $g_{out} = f(V_{DS})$ and transfer characteristics $I_{DS} = f(V_{GS})$ of our transistor as shown in Fig. 5, Fig. 6.

Finally, by observing the evolution of these characteristics, we can see that the larger channels present higher saturation currents and lower threshold voltages.

Fig. 1, Fig. 3, and Fig. 5 show the conductance $g_{out} = f(V_{DS})$ of the considered DG-SOI-MOSFET. The DG-SOI-MOSFET characteristics for all regions, linear, saturation and sub-threshold, can be generated from this continuous numeric solution.

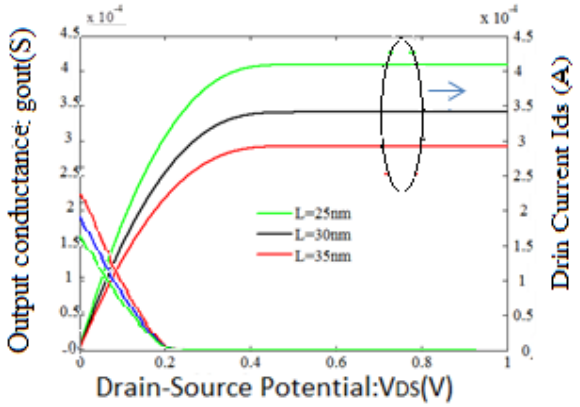


**Fig. 3** – Output characteristics and output conductance $I_{DS}$ and $g_{out}$ vs $V_{DS}$ for different channel length ($L$)

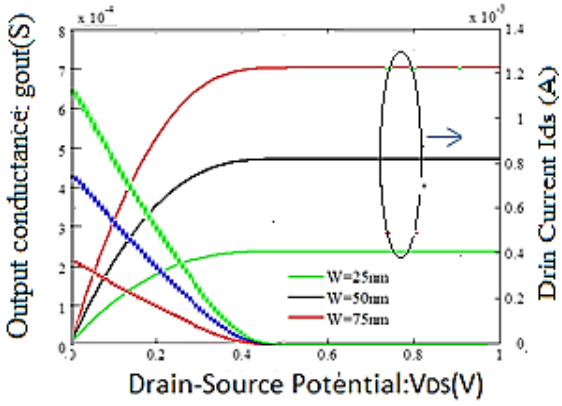


**Fig. 5** – Output characteristics and output conductance $I_{DS}$ and $g_{out}$ vs $V_{DS}$ for different channel width ($W$)

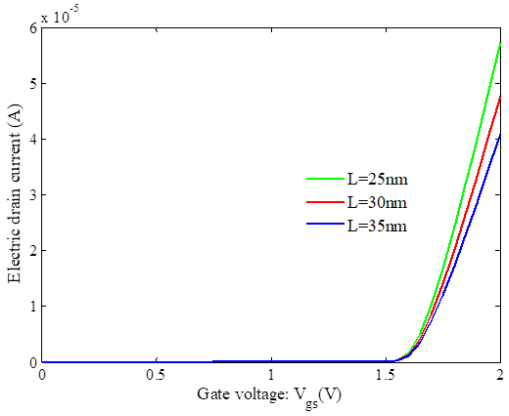


**Fig. 4** – Transfer characteristics $I_{DS} = f(V_{GS})$ for different channel length ($L$)

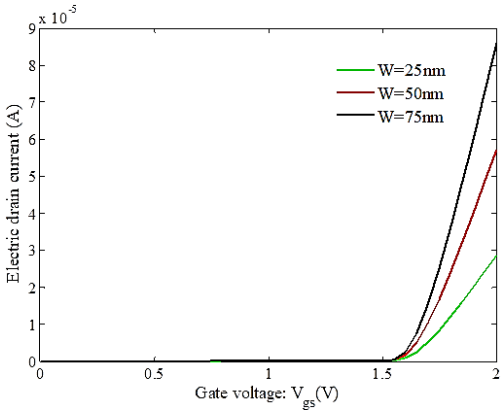


**Fig. 6** – Transfer characteristics $I_{DS} = f(V_{GS})$ for different channel width ($W$)

The inverse of the conductance ($1/g_d = R_{out}$) is a very important parameter in the design of analog circuits, where the output conductance ($g_d$) in saturation is characterized by the Early voltage ($V_{EA} = Id/g_d$).

We have tried to see the effect of the channel thickness by varying the thickness of 10, 20 and 30 nm, and we have deduced that the effect on these characteristics is less intense due to the weak direct proportionality with the saturation current and the very low linearity variation of the $I_{DS}$-$V_{GS}$ on a weak inversion. In general, our model agrees very well with the simulation results in the articles [11-13].

## 5. CONCLUSIONS

We have simulated the electrical characteristics and conductance for an undoped nanoscale symmetric double gate transistor using the graphical approach. We have seen the evolution of the output, transfer and output conductance characteristics by varying one of the three parameters of our component geometry, namely, channel length, channel width and oxide thickness. For component sizing to be reasonable, component miniaturization must be governed by the scale law. Possible use of DG-SOI-MOSFET technology makes it a suitable candidate for low power high performance circuits useful for applications in analogue and logic circuits, and radio frequency applications.

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# Вплив розмірів пристрою на електричні властивості DG-SOI-MOSFET за допомогою програмного забезпечення Octave

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Пристрій SOI-MOSFET із подвійним затвором (DG) розглядається як наступне покоління схем VLSI. У роботі ми показуємо вплив мініатюризації на попит та проблеми симетричної планарної конструкції DG-SOI-MOSFET низької потужності та високої продуктивності. Застосовуючи графічний підхід, який використовувався раніше і складається з чисельного моделювання, дійсного для всіх умов зсуву, від підпорогової до сильної інверсії та від лінійної до насичення, ми візуалізували еволюцію характеристик передачі, а також вихідних і електричних характеристик і вихідної провідності шляхом зміни кожного з параметрів незалежно: товщини оксиду ($t_{ox}$), довжини ($L$) і ширини каналу ($W$). Отримані результати дозволили перевірити, як кожен параметр впливає на різні електричні властивості DG-SOI-MOSFET. Було виявлено, що $L$, $W$ і $t_{ox}$ значним чином впливають на зазначені властивості, а даний транзистор також включає ефекти модуляції довжини каналу (CLM) та індуковане стоком зниження бар'єру (DIBL). Це дослідження показало здатність передбачити електричну поведінку DG-SOI-MOSFET за його геометричними розмірами та можливість вибору оптимальних розмірів для забезпечення високої продуктивності цього транзистора як в аналогових, так і в цифрових схемах.

**Ключові слова:** Симетричний DG-SOI-MOSFET, Електрична характеристика, Провідність, Мініатюризація, Чисельний метод.