JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. 16 No 2, 02010(5pp) (2024)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том 16 № 2, 02010(5cc) (2024)

REGULAR ARTICLE

A New GAA FinFET without *n*-well or *p*-well

A. Lazzaz[1,*], K. Bousbahi[1,2], M. Ghamnia[1]

[1] *Laboratoire des Sciences de la Matière Condensée (LSMC), Université d'Oran 1, Oran, Algérie*
[2] *École supérieure en génie électrique et énergétique (ESGEE), Oran, Algérie*

(Received 21 January 2024; revised manuscript received 19 April 2023; published online 29 April 2023)

The reduction in size of metal oxide semiconductor (MOS) devices results in the increase of leakage current due to Quantum effects. The different technologies proposed to overcome this problem. Variant structures of MOSFET such as Tri Gate FinFET or Pi gate and Omega gate to enhance current drive and control over the Short Channel Effects (SCE). In advanced technology node, the performance of CMOS circuits degrades. In sub 10 nm nodes technologies, FinFETs have a good channel control with high ON current (I_{ON}).Nowadays, power dissipation and leakage current are one the two crucial issues that the modern electronic industry is facing in 3 nm node technology. The other alternative devices such as novel GAA (Gate All Around) FinFET have been proposed to address these problems. This structure gained huge attention because of their possible fabrication process.In this paper, for the first time, we have investigated and simulated the different electrical characteristics of GAA FinFET 3 nm with N channel using HfO_2 (high k material oxide) to improve the subthreshold characteristics. In the second part of this paper, we present a novel correction for the equations used in this technology because no *n*-well layer is required anymore as the device channel is totally surrounded by the gate which enables the placement of n and p devices in a CMOS gate much closer to each other than previous technologies.

Keywords: FinFET, Quantum effect, Leakage current, CMOS.

DOI: 10.21272/jnep.16(2).02010 PACS numbers: 85.35.G, 85.30.T

1. INTRODUCTION

Since 1960s, MOSFET device scaling followed the development of new CMOS technology. The primary concern of downscaling MOS transistors is to maintain the electrostatic integrity of the device counteracting to Short Channel Effects (SCE), the design and the production of high-speed CMOS circuits, the reduction of production costs and the decrease of the power consumption [1-2].

The channel length with other critical parameters diminished with every new generation in order to enhance device performance, however, it generated different problems such as the increase of the threshold voltage VTH, the lowering of ON current and the enhancement of the Drain Induced Barrier Lowering (DIBL) [3].

To overcome these undesirable effects, multi gate structures such as Gate All Around (GAA) FinFET devices to enhance the electrostatic controllability of the gate.

The GAA FinFET offers the best electrostatic control of the channel since it cylindrical shape allows homogenous control and a tighter capacitive coupling to the device channel region from all directions, therefore a better control over SCE.

The increase of the leakage current from the quantum tunneling effect is due to the reduction of gate oxide. To overcome this problem, researchers in the nanoelectronics industry have proposed the use of high-*k* gate dielectrics.

The use of new oxides such as Hafnium Dioxide HfO_2 provides a high k dielectric material for the reduction of leakage current. It has a good lattice mismatch interface quality with silicon and a very good thermal and kinetic stability.

This work analyses in the first part a *p*-well GAA FinFET with 3 nm channel which is calibrated with experimental data. Different electrical characteristics are presented such as the transfer characteristics, transconductance and other calculated parameters.

The second part of this paper is to present a novel device of GAA FinFET without p well using mathematical corrections in the (I, V) characteristics produced with NEGF approach.

We explain the importance of the total capacitance in the new structure. The aim and the novelty of this paper is to compare the performance of both devices in order to have an optimal circuit and a good voltage transfer characteristic (VTC).

2. DEVICE AND PHYSICAL MODELS USED IN THIS SIMULATION

In this work, we have considered a 3D GAA FinFET structure in order to understand the effect of removing n and p well from the structure.

We have used the TCAD SILVACO ATLAS to draw

* Correspondence e-mail: lazzaz.abdelaziz@edu.univ-oran1.dz

© 2024 The Author(s). Journal of Nano- and Electronics Physics published by Sumy State University. This article is distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

Cite this article as: A. Lazzaz et al., *J. Nano- Electron. Phys.* 16 No 2, 02010 (2024) https://doi.org/10.21272/jnep.16(2).02010

the 3D structure as show in Fig. 1.

Different models are active in this simulation which comprises the drift diffusion transport approximation used for the carrier transport model, bandgap narrowing, Shockley-Read-Hall (SRH) recombination, concentration-dependent mobility, field-dependent mobility, velocity saturation and Auger recombination [13-17].

Figure 1 shows the structure used in this simulation. The dioxide used in this simulation is HfO_2 with dielectric constant equal to 24. The gate is highly doped with a work function of 4.05 eV [18].

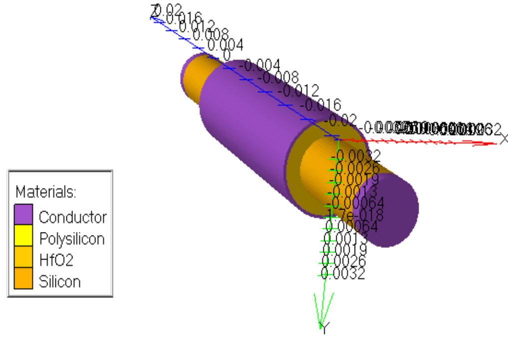

Fig. 1 – 3D GAA FinFET structure

In GAA FinFET devices, quantum effects have a large impact on their performance therefore, the simulation and modeling of quantum transport is important for many reasons such as the tunneling current through ultra-thin gate oxide and the increase of the threshold voltage.

The choice of different geometric and operating parameters are extracted from IRDS 2021 node [19] and PTM (Predictive Technology model) for the latest generation.

The NEGF provides the ability of solving Schrodinger equation and we start firstly from the usual time-independent Schrödinger equation [20]:

$$E(\psi) = |H|\{\Psi\} + |\Sigma|\{\Psi\} + \{S\} \tag{1}$$

H – Hamiltonian matrix whose eigenvalues represent the allowed energy levels and describe the quasiparticle dynamics around the equilibrium state.

Σ represents self-energy and it illustrates the disturbance from the open boundary conditions, it is included as part of the system Hamiltonian, $|\Sigma|\{\Psi\}$ and $\{s\}$ represent the out flow and inflow respectively.

Using the modified Schrödinger equation, the wave function can be written as the following equation:

$$\{\Psi\} = [EI - H - \Sigma]^{-1}\{s\} \tag{2}$$

I – is an identity matrix of the same size as the rest.

In order to remove the coherent in the source and to suppose multiple source, we define the following products as

$$G^R = [EI - H - \Sigma]^{-1} \tag{3}$$

$$G^A = [G^R]^+ \tag{4}$$

Therefore, we can write the wave function by the following equation:

$$\{\Psi\} = [G^R]\{S\} \tag{5}$$

So, we can define the NEGF equations as follows:

$$\{\Psi\}\{\Psi\}^+ = [G^R]\{s\}\{s\}^+[G^A] \tag{6}$$

$$G^n = G^R \Sigma^{in} G^A \tag{7}$$

Σ^{in} – in-scattering function.

The current equation of FinFET structure using NEGF formalism can *be* written as the following equation:

$$I^{op} = \frac{\sum G^n - G^n \Sigma^+}{i} + \frac{\Sigma^{in} G^A - G^R \Sigma^{in}}{i} \tag{8}$$

$\hbar$ – plank constant, Σ – out flow, Σ^{in} – in-scattering function.

In the subthreshold region, the drain current can be expressed by the following expression [15]:

$$I_{DS} \approx \frac{\mu}{L_G} \upsilon_T{}^2 C_{inv} \exp\left(\frac{V_g - V_{th}}{\gamma \upsilon_T}\right)\left(1 - \exp\left(\frac{-V_{BS}}{V_T}\right)\right) \tag{9}$$

C_{ins} is the insulator capacitance, V_T is the equivalent thermal temperature, V_{DS} is the applied drain-to-source voltage, V_{TH} is the threshold voltage, μ – electron mobility and γ is the body factor.

The threshold voltage V_{TH} is a very important parameter for obtaining the ON current. The threshold voltage is represented by the following equation [5]:

$$V_{TH} = \varphi_{ms} + 2\varphi_F + \frac{Q_D}{C_{OX}} + \frac{Q_{SS}}{C_{OX}} + V_{in} \tag{10}$$

Q_{SS} – Charge in the gate dielectric, C_{OX} – gate capacitance, Q_D – depletion charge, φ_F – Fermi potential with respect to the conduction band minimum, V_{in} – input voltage.

The Fermi potential for N type silicon is:

$$\varphi_F = \left(\frac{k_B T}{q}\right)\ln\left(\frac{np}{n_i{}^2}\right) \tag{11}$$

k_B – Boltzmann constant, T – temperature, n – electron density, n_i – intrinsic carrier concentration, p – minority hole density.

The subthreshold slope (SS) is a major parameter for calculating the leakage current and is expressed as [9]:

$$SS = \frac{dV_{GS}}{d(\log_{10} I_{DS})} \tag{12}$$

The value of the Drain Induced Barrier Lowering (DIBL) is calculated by the following relation [4]:

$$DIBL = \frac{dV_{TH}}{dV_{DS}} \tag{13}$$

3. RESULTS

Below 5 nm technology node, there are only 2 to 20 grains on the surface of the gate electrode therefore, highly doped polysilicon material (10^{20}cm^{-3}) has been used to overcome this problem [21].

The first step of the simulation is to calibrate the model used in this simulation. Table 1 displays all the key geometric parameters of the device structure used in this simulation.

Table 1 – Geometric parameters

Symbol	Quantity	Values
L	Channel length	3 nm
L_G	Gate length	8 nm
d	diameter	6.4 nm
L_D/L_S	Drain/Source length	10 nm

Table 2 – Operating parameters

Symbol	Quantity	Values
N_{CH}	Channel concentration	10^{16} cm^{-3}
t_{ox}	Gate length	0.5 nm
N_S/N_D	Source/Drain concentration	10^{20} cm^{-3}
V_{DD}	Supply voltage	0.65 V

Figure 2 shows the calibrated *I-V* and transfer characteristics of the device in logarithm scale. We note that the gate voltage is swept from 0 V to 1 V.

The ON current represents the drain current with $V_{GS} = V_{DD}$ and its value in this simulation is 10^{-4} A/µm.

The results obtained using this physical model is compared with the experimental data [12]. We note a good agreement in the saturation regime. Lowering the channel length increases the threshold voltage V_{TH} but this leads to quantum short channel effect which oppose the V_{TH} enhancement.

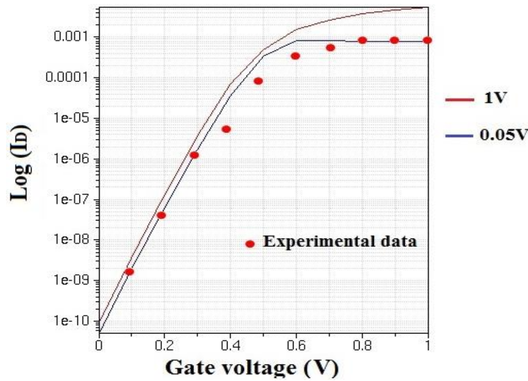

Fig. 2 – Fitting of Simulated curve with experimental data in GAA FinFET 3 nm channel length [12]

We note that the experimental data fit with good convergence for gate voltage higher than 0.65 V and in order to improve the accuracy of the Drift-Diffusion equations (DD) on complex device structures some quantum corrections cannot be ignored anymore for (*I*, *V*) characteristic on the subthreshold regime.

Table 3 displays the performance parameters and a comparison with IRDS model of 3 nm node technology. The aim of this comparison is to compare the performance model with different models in the Nano technology industry [23].

Table 3 – Performance parameters

Symbol	Quantity	Values
I_{ON}	ON current	5.55×10^{-3} (A/µm)
I_{OFF}	Leakage current	5.18×10^{-11} (A/µm)
I_{ON}/I_{OFF}	Performance ratio	1.07×10^{-8}
SS	Subthreshold slope	77.94 (mV/dec)
V_{TH}	Threshold voltage	0.44 V

We note from the results illustrate in the table III that the increase of the threshold voltage is due to the increase of the fermi level. To minimize the threshold voltage, we increase the Fin height.

The optimal value of the subthreshold slope (SS) is 60 mV/dec and the decrease the total capacitance decreases the SS value.

Figure 3 illustrates the transconductance of the device, the gate voltage is swept from 0 V to 1 V with $V_{DS} = 0.05$ V and 1 V [16].

The larger value of the transconductance can be explained by the higher strain in the short channel device due the miniaturization of the channel length. We can reduce the peak value of the transconductance by the reduction of the channel length. Shorter gate length L_G provides less resistance and lower surface-roughness scattering which leads to a higher transconductance and mobility.

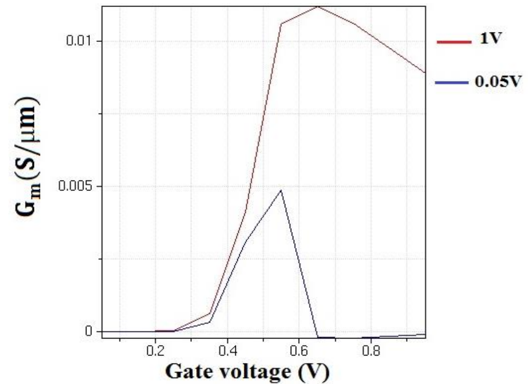

Fig. 3 – Simulated curve of GAA FinFET 3 nm channel length

Gate capacitance model can be used for GAA FinFET to compute the drain current. A comprehensive approach is used by solving Poisson's equation in order to obtain current values equation.

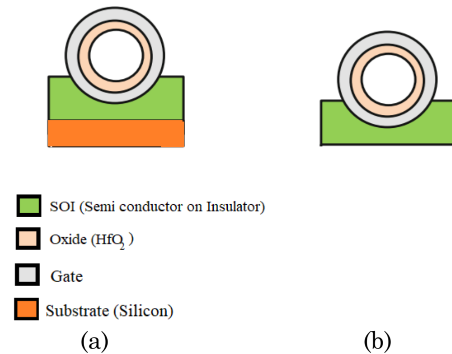

Fig. 4 – New GAA FinFET with and without *p*-well

In this section, we present a new structure of GAA FinFET 3 nm without *p*-well.

We note that both structures are implemented on the Semiconductor on insulator (SOI). The active thin body is on silicon oxide which is a good thermal insulator.

Figure 4 shows both structures: a) *p*-well GAA FinFET and (b) GAA FinFET without *p*-well.

The subthreshold swing is computed from the values of the internal capacitances of the device. In the device without *p*-well, the SS values decrease because of the reduction of total capacitance as the substrate is removed [9-14].

To have the (*I*, *V*) characteristics for the new structure without *p*-well, we proposed a correction factor to modify the model.

The first step in this mathematical correction is to calculate the new body factor of GAA FinFET without p well and second the step is to extract the drain current characteristics from the following equation [15]:

$$I_{DS(without-p-well)} = CF \times I_{DS} \quad (14)$$

CF – correction factor.

Figure 5 shows the drain currents of both structures. The gate voltage is swept from 0 to 1 V for $V_{DS} = 1$ V. The operating parameters used in this simulation are presented in Table 2.

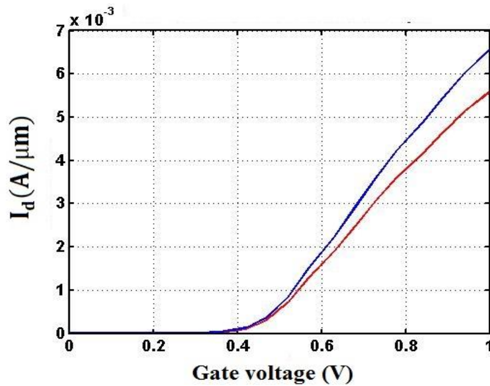

Fig. 5 – GAA FinFET with *p*-well (red color), GAA FinFET without *p*-well (blue color)

We note that the ON current of the GAA FinFET without p well is 6.56×10^{-3}A/μm. It is high because of the reduction of the strain effect. From table IV notice that the leakage current of GAA FinFET without *p*-well is 2.12 % lower than that of GAA FinFET with *p*-well.

The results confirm that leakage current issues can be solved by GAA FinFET 3 nm with *N* channel using HfO_2 without *p*-well.

Strain effect enhance band banding at the interface semiconductor-insulator and therefore enhances tunneling current. The choice of the geometric parameters such as the gate oxide length can lead to the raising of the conduction band, and therefore, more potential in needed to create an inversion layer [5]-[10]-[22]. Table 4 displays performance parameters of both devices with 3 nm channel length.

Table 4 – Performance parameters

Parameters	GAA FinFET with *p*-well	GAA FinFET without *p*-well
I_{ON} (A/μm)	5.55×10^{-3}	6.56×10^{-3}
I_{OFF} (A/μm)	5.18×10^{-11}	5.07×10^{-11}
I_{ON}/I_{OFF}	1.07×10^{8}	1.29×10^{8}
SS (mV/dec)	77.94	60.05
Power dissipation (W)	1.01×10^{-13}	0.98×10^{-13}

The subthreshold swing calculated with GAA FinFET without p well is higher than that obtained with Vinay Vashishtha et al [11].

The simulation results of the new structure confirm that the ON current is higher than that calculated by Uttam Kumar Das [8].

According to the results obtained in our characterization, we note that the performance ratio must be higher than 10^6 [7]. In this simulation, we note that the performance ratio is higher than 10^6 therefore, both structures are a good candidate as devices for circuits applications.

We conclude that GAA FinFET without *p*-well is more efficient because it has a higher performance ratio I_{ON}/I_{OFF} [6].

4. CONCLUSION

To summarize a GAA FinFET with 3 nm channel length is investigated by taking into consideration quantum effects and quantum transport. The (*I*, *V*) characteristics are verified using experimental data.

A new structure GAA FinFET without *p*-well has been proposed and simulated and a comparison has been done between both devices. The results of the simulations confirm that the two structures can be a good device for circuits applications. GAA FinFET without p well has a slightly higher performance ratio than that of GAA FinFET with *p*-well. Our results show that using the device without *p*-well allows a reduction of the subthreshold swing as the total capacitance decreases.

AKNOWLEDGEMENTS

The authors wish to thank Prof. Etienne Sicard and Prof. Pierpaolo Palestri for their helpful suggestions in the accomplishment of this work.

REFERENCES

1. A. Razavieh, P. Zeitzoff, E. Nowak, *J. IEEE Trans. Nanotechnol.* **18**, 999 (2009).
2. T. Pešić-Brđanin, B. Dokić, *J. Electron.* **18** No 2, 63 (2014).
3. A. Kumar, S. Saini, A. Gupta, N. Gupta, M. Tripathi, R. Chaujar, *2020 6th International Conference on Signal Processing and Communication (ICSC),* 310 (2020).
4. A. Lazzaz, K. Bousbahi , M. Ghamnia, *2021 IEEE 21st International Conference on Nanotechnology (NANO)- IEEE,* 177 (2021).
5. A. Lazzaz, K. Bousbahi, Ghamnia, *J. Micro Nanostruct.* 207210 (2022).
6. E. Sicard, L. Trojman, I. Vanves, *Introducing 3-nm Nano-*

Sheet FET Technology in Microwind (2021).
7. Y. Eng, L. Hu, T. Chang, S. Hsu, C. Chiou, T. Wang, M. Chang, *J. IEEE J. Electron Dev. Soc.* **6**, 207 (2018).
8. U. Das, U. Kumar, Bhattacharyya, Tarun Kanti, *J. IEEE Trans. Electron Dev.* **67** No 6, 2633 (2020).
9. M. Lundstrom, *Fundamentals of Nano Transistors* (World Scientific Publishing Company: 2017).
10. Y. Chauhan, D. Lu, S. Venugopalan, S. Khandelwal, J. Duarte, N. Paydavosi, C. Hu, *FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard* (Academic Press: 2015).
11. V. Vashishtha, L. Clark, T. Lawrence, *Microelectron. J.* **107**, 104942 (2021).
12. T. Dash, S. Dey, S. Das, *J. Physica E: Low-dimensional Systems and Nanostructures* **118**, 113964 (2020).
13. B. Kumar, R. Chaujar, *Silicon* **13** No 10, 3741 (2021).
14. A. Es-Sakhi, M. Chowdhury, *Microelectron. J.* **62**, 30 (2017).
15. A. Dixit, D. Samajdar, *J. Appl. Phys. A* **126** No 10, 782 (2020).
16. R. Saha, B. Bhowmick, S. Baishya, *Indian J. Phys.* **95** No 11, 2387 (2021).
17. N. Bourahla, A. Bourahla, B. Hadri, *Indian J. Phys.* **95** No 10, 1977 (2021).
18. M. Rau, E. Caruso, D. Lizzit, *2016 IEEE International Electron Devices Meeting (IEDM)*, 30 (2016).
19. https://irds.ieee.org (2021 Edition).
20. S. Datta, *2015 International Workshop on Computational Electronics (IWCE)*, 1 (2015)
21. K. Ko, M. Kang, J. Jeon, *J. IEEE Trans. Electron Dev.* **66** No 3, 1613 (2019).
22. A. Lazzaz, K. Bousbahi, M. Ghamnia, *2023 27th International Conference on Information Technology (IT)*, 1 (2023).
23. A. Lazzaz, K. Bousbahi, M. Ghamnia, *J. Nano- Electron. Phys.* **15** No 2, 02005 (2023).

Новий транзистор GAA FinFET без *n*- і *p*-каналів

A. Lazzaz[1], K. Bousbahi[1,2], M. Ghamnia[1]

[1] *Laboratoire des Sciences de la Matière Condensée (LSMC), Université d'Oran 1, Oran, Algérie*
[2] *École supérieure en génie électrique et énergétique (ESGEE), Oran, Algérie*

Зменшення розміру метал-окисел-напівпровідник (МОН) пристроїв призводить до збільшення витоку струму через квантові ефекти. Різні технології, запропоновані для подолання цієї проблеми. Варіант структур MOSFET, таких як Tri Gate FinFET або Pi gate і Omega gate для посилення струмового приводу та контролю над ефектами короткого каналу (SCE). У передових технологічних вузлах продуктивність схем CMOS погіршується. У технологіях вузлів нижче 10 нм польові транзистори мають хороший контроль каналу з високим струмом ввімкнення. Зараз розсіювання потужності та струм витоку є однією з двох ключових проблем, з якими стикається сучасна електронна промисловість у технології вузлів 3 нм. Інші альтернативні пристрої, такі як новий польовий транзистор GAA (Gate All Around), були запропоновані для вирішення цих проблем. Структура привернула увагу через можливий процес їх виготовлення. У цій статті вперше досліджено та змодельовано різні електричні характеристики польового транзистора з n-каналом HfO_2 для покращення підпорогового значення. характеристики. Запропонована нова поправка для рівнянь, що використовуються в цій технології, оскільки більше не потрібний шар з n-лунками, оскільки канал пристрою повністю оточений затвором, що дозволяє розміщувати n- та p-пристрої в CMOS набагато ближче один до одного, ніж в попередніх технологіях.

Ключові слова: Польовий транзистор, Квантовий ефект, Струм витоку, КМОН.